# F<sup>2</sup>MC-8FX 8-BIT MICROCONTROLLER MB95130/M Series HARDWARE MANUAL



# F<sup>2</sup>MC-8FX 8-BIT MICROCONTROLLER MB95130/M Series HARDWARE MANUAL

Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

**FUJITSU LIMITED** 

# PREFACE

#### The Purpose and Intended Readership of This Manual

Thank you very much for your continued special support for Fujitsu semiconductor products.

The MB95130/M series is a line of products developed as general-purpose products in the  $F^2MC-8FX$  series of proprietary 8-bit single-chip microcontrollers applicable as application-specific integrated circuits (ASICs). The MB95130/M series can be used for a wide range of applications from consumer products including portable devices to industrial equipment.

Intended for engineers who actually develop products using the MB95130/M series of microcontrollers, this manual describes its functions, features, and operations. You should read through the manual.

For details on individual instructions, refer to the "F<sup>2</sup>MC-8FX Programming Manual".

Note: F<sup>2</sup>MC is the abbreviation of FUJITSU Flexible Microcontroller.

#### Trademark

The company names and brand names in this document are the trademarks or registered trademarks of their respective owners.

#### Sample Programs

Fujitsu provides sample programs free of charge to operate the peripheral resources of the  $F^2MC-8FX$  family of microcontrollers. Feel free to use such sample programs to check the operational specifications and usages of Fujitsu microcontrollers.

Microcontroller support information:

http://www.fujitsu.com/global/services/microelectronics/product/micom/support/

Note that sample programs are subject to change without notice. As these pieces of software are offered to show standard operations and usages, evaluate them sufficiently before use with your system. Fujitsu assumes no liability for any damages whatsoever arising out of the use of sample programs.

 The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

- The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
- Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
- The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite). Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
- Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
- If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

Copyright ©2006 FUJITSU LIMITED All rights reserved.

# CONTENTS

СНАРТ	ER 1	DESCRIPTION	1
1.1	Feature	e of MB95130/M Series	
1.2	Produc	t Lineup of MB95130/M Series	4
1.3	Differe	nce Points among Products and Notes on Selecting a Product	6
1.4	Block D	Diagram of MB95130/M Series	
1.5	Pin Ass	signment	
1.6	Packad	ge Dimension	10
1.7	Pin De	scription	11
1.8	I/O Ciro	cuit Type	13
СНАРТ	ER 2	HANDLING DEVICES	15
2.1	Device	Handling Precautions	16
СНАРТ	ER 3	MEMORY SPACE	21
3.1	Memor	v Space	22
3.1.1	Area	as for Specific Applications	24
3.2	Memor	y Map	25
СНАРТ	FR 4	MEMORY ACCESS MODE	27
4.1	Memor	y Access Mode	
спурт		CDU	20
5 1		CFOtod Pagistara	20
5.1	Deuica	victor Rank Dointor (PD)	
5.1.1		pister Bark Pointer (NP)	
5.1.2		odition Code Register (CCP)	
5.1.3	Gonore	Nation Code Register (CCR)	
5.Z	Diego	ar-purpose Registers	
5.3	Placem	ient of 16-bit Data in Memory	
CHAPT	ER 6	CLOCK CONTROLLER	41
6.1	Overvie	ew of Clock Controller	42
6.2	Oscillat	tion Stabilization Wait Time	48
6.3	System	n Clock Control Register (SYCC)	50
6.4	PLL Co	ontrol Register (PLLC)	52
6.5	Oscillat	tion Stabilization Wait Time Setting Register (WATR)	55
6.6	Standb	y Control Register (STBC)	58
6.7	Clock N	Modes	61
6.8	Operat	ions in Low-power Consumption Modes (Standby Modes)	66
6.8.1	Note	es on Using Standby Mode	67
6.8.2	Slee	ep Mode	71
6.8.3	Stop	p Mode	72
6.8.4	. Tim	ebase Timer Mode	73

6.8.5	Watch Mode	
6.9	Clock Oscillator Circuits	75
6.10	Overview of Prescaler	77
6.11	Configuration of Prescaler	
6.12	Operating Explanation of Prescaler	
6.13	Notes on Use of Prescaler	80
CHAPTI	ER 7 RESET	81
7.1	Reset Operation	
7.2	Reset Source Register (RSRR)	
CHAPTI	ER 8 INTERRUPTS	89
8.1	Interrupts	
8.1.1	Interrupt Level Setting Registers (ILR0 to ILR5)	
8.1.2	Interrupt Processing	
8.1.3	Nested Interrupts	
8.1.4	Interrupt Processing Time	
8.1.5	Stack Operations During Interrupt Processing	
8.1.6	Interrupt Processing Stack Area	
СНАРТІ	ER 9 I/O PORT	
9.1	Overview of I/O Ports	100
9.2	Port 0	101
9.2.1	Port 0 Registers	104
9.2.2	Operations of Port 0	105
9.3	Port 1	107
9.3.1	Port 1 Registers	109
9.3.2	Operations of Port 1	110
9.4	Port F	112
9.4.1	Port F Registers	114
9.4.2	Operations of Port F	
9.5	Port G	117
9.5.1	Port G Registers	
9.5.2	Operations of Port G	120
CHAPTI	ER 10 TIMEBASE TIMER	123
10.1	Overview of Timebase Timer	124
10.2	Configuration of Timebase Timer	125
10.3	Registers of the Timebase Timer	127
10.3.	1 Timebase Timer Control Register (TBTC)	128
10.4	Interrupts of Fimebase Timer	
10.5	Explanation of Limebase Limer Operations and Setup Procedure Example	
10.6	Precautions when Using Limebase Limer	135
CHAPTI	ER 11 WATCHDOG TIMER	137
11.1	Overview of Watchdog Timer	138
11.2	Configuration of Watchdog Timer	139

11.3	Registers of the Watchdog Timer	141
11.3	.1 Watchdog Timer Control Register (WDTC)	142
11.4	Explanation of Watchdog Timer Operations and Setup Procedure Example	144
11.5	Precautions when Using Watchdog Timer	146
СНАРТ	ER 12 WATCH PRESCALER	147
12.1	Overview of Watch Prescaler	148
12.2	Configuration of Watch Prescaler	149
12.3	Registers of the Watch Prescaler	151
12.3	.1 Watch Prescaler Control Register (WPCR)	152
12.4	Interrupts of Watch Prescaler	154
12.5	Explanation of Watch Prescaler Operations and Setup Procedure Example	156
12.6	Precautions when Using Watch Prescaler	158
12.7	Sample Programs for Watch Prescaler	159
СНАРТ	ER 13 WATCH COUNTER	161
13.1	Overview of Watch Counter	
13.2	Configuration of Watch Counter	163
13.3	Registers of Watch Counter	165
13.3	.1 Watch Counter Data Register (WCDR)	166
13.3	.2 Watch Counter Control Register (WCSR)	167
13.4	Interrupts of Watch Counter	169
13.5	Explanation of Watch Counter Operations and Setup Procedure Example	170
13.6	Precautions when Using Watch Counter	172
13.6 13.7	Precautions when Using Watch Counter Sample Programs for Watch Counter	172 173
13.6 13.7 CHAPT	Precautions when Using Watch Counter Sample Programs for Watch Counter ER 14 WILD REGISTER	172 173 <b>175</b>
13.6 13.7 <b>CHAPT</b> 14.1	Precautions when Using Watch Counter	172 173 <b>175</b> 176
13.6 13.7 <b>CHAPT</b> 14.1 14.2	Precautions when Using Watch Counter	172 173 <b>175</b> 176 177
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3	Precautions when Using Watch Counter	172 173 175 176 177 179
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3	Precautions when Using Watch Counter	172 173 175 176 177 179 181
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3	Precautions when Using Watch Counter	172 173 175 176 177 179 181 182
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3	Precautions when Using Watch Counter	172 173 175 176 177 179 181 182 183
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3	Precautions when Using Watch Counter	
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.3 14.3	Precautions when Using Watch Counter	
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.3 14.4 14.5	Precautions when Using Watch Counter	172 173 175 176 177 179 181 182 183 184 185 186
13.6 13.7 CHAPT 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 CHAPT	Precautions when Using Watch Counter	172 173 173 175 176 177 179 181 182 183 184 185 187
13.6 13.7 CHAPT 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 CHAPT 15.1	Precautions when Using Watch Counter	172 173 173 176 176 177 179 181 182 183 186 187 188
13.6 13.7 CHAPT 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 CHAPT 15.1 15.2	Precautions when Using Watch Counter	172 173 173 176 176 177 179 181 182 183 186 188 188 188
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3	Precautions when Using Watch Counter	172 173 173 176 176 176 177 179 181 182 183 186 186 188 188 190 193
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3 15.4	Precautions when Using Watch Counter	
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3 15.4 15.5	Precautions when Using Watch Counter	
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3 15.4 15.5	Precautions when Using Watch Counter	
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3 15.4 15.5 15.5	Precautions when Using Watch Counter	172 173 173 176 176 177 179 181 182 183 184 185 186 188 188 190 193 194 197 200
13.6 13.7 <b>CHAPT</b> 14.1 14.2 14.3 14.3 14.3 14.3 14.3 14.4 14.5 <b>CHAPT</b> 15.1 15.2 15.3 15.4 15.5 15.5 15.5	Precautions when Using Watch Counter	

	15.6	Interrupts of 8/16-bit Compound Timer	209
	15.7	Operating Description of Interval Timer Function (One-shot Mode)	211
	15.8	Operating Description of Interval Timer Function (Continuous Mode)	213
	15.9	Operating Description of Interval Timer Function (Free-run Mode)	215
	15.10	Operating Description of PWM Timer Function (Fixed-cycle mode)	217
	15.11	Operating Description of PWM Timer Function (Variable-cycle Mode)	219
	15.12	Operating Description of PWC Timer Function	221
	15.13	Operating Description of Input Capture Function	223
	15.14	Operating Description of Noise Filter	225
	15.15	States in Each Mode during Operation	226
	15.16	Precautions when Using 8/16-bit Compound Timer	228
С	НАРТЕ	-R 16 8/16-BIT PPG	229
•	16 1	Overview of 8/16-bit PPG	230
	16.1	Configuration of 8/16-bit PPG	231
	16.3	Channels of 8/16-bit PPG	233
	16.0	Pins of 8/16-bit PPG	234
	16.5	Registers of 8/16-bit PPG	236
	16.5.1	8/16-bit PPG Timer 01 Control Register ch.0 (PC01)	237
	16.5.2	2 8/16-bit PPG Timer 00 Control Register ch.0 (PC00)	239
	16.5.3	8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register (PPS01/PPS00)	241
	16.5.4	4 8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/PDS00)	242
	16.5.5	5 8/16-bit PPG Start Register (PPGS)	243
	16.5.6	6 8/16-bit PPG Output Inversion Register (REVC)	244
	16.6	Interrupts of 8/16-bit PPG	245
	16.7	Operating Description of 8/16-bit PPG	246
	16.7.1	1 8-bit PPG Independent Mode	247
	16.7.2	2 8-bit Prescaler + 8-bit PPG Mode	249
	16.7.3	3 16-bit PPG Mode	251
	16.8	Precautions when Using 8/16-bit PPG	253
	16.9	Sample Programs for 8/16-bit PPG Timer	254
C	НАРТЕ	R 17 16-BIT PPG TIMER	257
	17 1	Overview of 16-bit PPG Timer	258
	17.2	Configuration of 16-bit PPG Timer	259
	17.3	Channels of 16-bit PPG Timer	261
	17.4	Pins of 16-bit PPG Timer	262
	17.5	Registers of 16-bit PPG Timer	263
	17.5.1	1 16- bit PPG Down Counter Registers (PDCRH0, PDCRL0)	264
	17.5.2	2 16-bit PPG Cycle Setting Buffer Registers (PCSRH0, PCSRL0)	265
	17.5.3	3 16-bit PPG Duty Setting Buffer Registers (PDUTH0. PDUTL0)	266
	17.5.4	4 16-bit PPG Status Control Register (PCNTH0. PCNTL0)	267
	17.6	Interrupts of 16-bit PPG Timer	271
	17.7	Explanation of 16-bit PPG Timer Operations and Setup Procedure Example	272
	17.8	Precautions when Using 16-bit PPG Timer	276
	17.9	Sample Programs for 16-bit PPG Timer	277
		· · ·	

CU1	ER 18 EXTERNAL INTERRUPT CIRCUIT	281
1	Overview of External Interrupt Circuit	282
1	Configuration of External Interrupt Circuit	283
1	Channels of External Interrupt Circuit	284
1	Pins of External Interrupt Circuit	285
1	Registers of External Interrupt Circuit	286
	5.1 External Interrupt Control Register (EIC00)	287
1	Interrupts of External Interrupt Circuit	289
1	Explanation of External Interrupt Circuit Operations and Setup Procedure Example	290
1	Precautions when Using External Interrupt Circuit	292
1	Sample Programs for External Interrupt Circuit	293
СН	FER 19 INTERRUPT PIN SELECTION CIRCUIT	295
1	Overview of Interrupt Pin Selection Circuit	296
1	Configuration of Interrupt Pin Selection Circuit	297
1	Pins of Interrupt Pin Selection Circuit	298
1	Registers of Interrupt Pin Selection Circuit	299
	1.1 Interrupt Pin Selection Circuit Control Register (WICR)	300
1	Operating Description of Interrupt Pin Selection Circuit	303
1	Precautions when Using Interrupt Pin Selection Circuit	304
СН	TER 20 UART/SIO	305
2	Overview of UART/SIO	306
2	Configuration of UART/SIO	307
2 2	Configuration of UART/SIO Channels of UART/SIO	307 309
2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO	307 309 310
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO	307 309 310 312
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10)	307 309 310 312 313
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20)	<ol> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> </ol>
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0)	<ol> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> </ol>
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0)	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> </ul>
2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO UART/SIO Serial Mode Control Register 1 (SMC10) UART/SIO Serial Mode Control Register 2 (SMC20) UART/SIO Serial Status and Data Register (SSR0) UART/SIO Serial Input Data Register (RDR0) UART/SIO Serial Output Data Register (TDR0)	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> </ul>
2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (TDR0) Interrupts of UART/SIO	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> </ul>
2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> </ul>
2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (TDR0) Interrupts of UART/SIO Explanation of UART/SIO Operations and Setup Procedure Example	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> </ul>
2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Mode Control Register (SSR0) 5.4 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (TDR0) Interrupts of UART/SIO Explanation of UART/SIO Operations and Setup Procedure Example 7.1 Operating Description of Operation Mode 0	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> </ul>
2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (TDR0) Interrupts of UART/SIO Operations and Setup Procedure Example 7.1 Operating Description of Operation Mode 0 7.2 Operating Description of Operation Mode 1 Sample Programs for UART/SIO FER 21 UART/SIO DEDICATED BAUD RATE GENERATOR	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Status and Data Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (TDR0) Interrupts of UART/SIO Explanation of UART/SIO Operations and Setup Procedure Example 7.1 Operating Description of Operation Mode 0 7.2 Operating Description of Operation Mode 1 Sample Programs for UART/SIO FER 21 UART/SIO DEDICATED BAUD RATE GENERATOR Overview of UART/SIO Dedicated Baud Rate Generator	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> <li>342</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> <li>342</li> <li>343</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 5.1 UART/SIO Serial Mode Control Register 1 (SMC10) 5.2 UART/SIO Serial Mode Control Register 2 (SMC20) 5.3 UART/SIO Serial Mode Control Register (SSR0) 5.4 UART/SIO Serial Input Data Register (RDR0) 5.5 UART/SIO Serial Output Data Register (RDR0) Interrupts of UART/SIO Explanation of UART/SIO Operations and Setup Procedure Example 7.1 Operating Description of Operation Mode 0 7.2 Operating Description of Operation Mode 1 Sample Programs for UART/SIO FIER 21 UART/SIO DEDICATED BAUD RATE GENERATOR Overview of UART/SIO Dedicated Baud Rate Generator Channels of UART/SIO Dedicated Baud Rate Generator Registers of UART/SIO Dedicated Baud Rate Generator Registers of UART/SIO Dedicated Baud Rate Generator	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> <li>342</li> <li>343</li> <li>344</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO Channels of UART/SIO Pins of UART/SIO Registers of UART/SIO 	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> <li>342</li> <li>343</li> <li>344</li> <li>345</li> </ul>
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Configuration of UART/SIO	<ul> <li>307</li> <li>309</li> <li>310</li> <li>312</li> <li>313</li> <li>315</li> <li>317</li> <li>319</li> <li>320</li> <li>321</li> <li>322</li> <li>323</li> <li>330</li> <li>336</li> <li>341</li> <li>342</li> <li>343</li> <li>344</li> <li>345</li> <li>346</li> </ul>

СНАРТ	ER 22 LIN-UART	. 349
22.1	Overview of LIN-UART	350
22.2	Configuration of LIN-UART	352
22.3	LIN-UART Pins	357
22.4	Registers of LIN-UART	358
22.4	L1 LIN-UART Serial Control Register (SCR)	359
22.4	LIN-UART Serial Mode Register (SMR)	361
22.4	I.3 LIN-UART Serial Status Register (SSR)	363
22.4	LIN-UART Reception Data Register/LIN-UART Transmit Data Register (RDR/TDR)	365
22.4	LIN-UART Extended Status Control Register (ESCR)	367
22.4	6 LIN-UART Extended Communication Control Register (ECCR)	369
22.4	LIN-UART Baud Rate Generator Register 0, 1 (BGR 0/1)	371
22.5	LIN-UART Interrupt	372
22.5	5.1 Timing of Reception Interrupt Generation and Flag Set	376
22.5	5.2 Timing of transmit interrupt generation and flag set	378
22.6	LIN-UART Baud Rate	380
22.6	6.1 Baud Rate Setting	382
22.6	6.2 Reload Counter	386
22.7	Operations and Setting Procedure Example of LIN-UART	388
22.7	7.1 Operation of Asynchronous Mode (Operation Mode 0, 1)	390
22.7	7.2 Operation of Synchronous Mode (Operation Mode 2)	394
22.7	Constraint         Constrait         Constrait         Constrait	398
22.7	7.4 Serial Pin Direct Access	401
22.7	7.5 Bidirectional Communication Function (Normal Mode)	402
22.7	7.6 Master/Slave Mode Communication Function (Multiprocessor Mode)	404
22.7	2.7 LIN Communication Function	407
22.7	7.8 Example of LIN-UART LIN Communication Flowchart (Operation Mode 3)	408
22.8	Notes on Using LIN-UART	410
22.9	Sample Programs of LIN-UAR I	412
СНАРТ	ER 23 8/10-BIT A/D CONVERTER	. 417
23.1	Overview of 8/10-bit A/D Converter	418
23.2	Configuration of 8/10-bit A/D Converter	419
23.3	Pins of 8/10-bit A/D Converter	421
23.4	Registers of 8/10-bit A/D Converter	423
23.4	1 8/10-bit A/D Converter Control Register 1 (ADC1)	424
23.4	8/10-bit A/D Converter Control Register 2 (ADC2)	426
23.4	8/10-bit A/D Converter Data Registers Upper/Lower (ADDH, ADDL)	428
23.5	Interrupts of 8/10-bit A/D Converter	429
23.6	Operations of 8/10-bit A/D Converter and Its Setup Procedure Examples	430
23.7	Notes on Use of 8/10-bit A/D Converter	433
23.8	Sample Programs for 8/10-bit A/D Converter	434

CHAPTER 24 LOW-VOLTAGE DETECTION RESET CIRCUIT	437
24.1 Overview of Low-voltage Detection Reset Circuit	438
24.2 Configuration of Low-voltage Detection Reset Circuit	439
24.3 Pins of Low-voltage Detection Reset Circuit	440
24.4 Operations of Low-voltage Detection Reset Circuit	441
CHAPTER 25 256-KBIT FLASH MEMORY	443
25.1 Overview of 256-Kbit Flash Memory	444
25.2 Sector Configuration of Flash Memory	445
25.3 Register of Flash Memory	446
25.3.1 Flash Memory Status Register (FSR)	447
25.4 Starting the Flash Memory Automatic Algorithm	449
25.5 Checking the Automatic Algorithm Execution Status	451
25.5.1 Data Polling Flag (DQ7)	453
25.5.2 Toggle Bit Flag (DQ6)	454
25.5.3 Execution Time-out Flag (DQ5)	455
25.5.4 Toggle Bit 2 Flag (DQ2)	456
25.6 Details of Programming/Erasing Flash Memory	457
25.6.1 Placing Flash Memory in the Read/Reset State	458
25.6.2 Programming Data into Flash Memory	459
25.6.3 Erasing All Data from Flash Memory (Chip Erase)	461
25.7 Features of Flash Security	462
CHAPTER 26 EXAMPLE OF SERIAL PROGRAMMING CONNECTION	463
26.1 Basic Configuration of MB95F136MS, NS/MW, NW Serial Programming Connection	464
26.2 Example of Serial Programming Connection	467
26.3 Example of Minimum Connection to Flash Microcomputer Programmer	469
APPENDIX	471
APPENDIX A I/O Map	472
APPENDIX B Table of Interrupt Causes	476
APPENDIX C Memory Map	477
APPENDIX D Pin Status of MB95130/M series	479
APPENDIX E Instruction Overview	481
APPENDIX F Mask Option	497
APPENDIX G Writing to Flash Microcontroller Using Parallel Writer	499
Index	501
Register Index	525
Pin Function Index	527

# Main changes in this edition

Page	Changes (For details, refer to main body.)
-	First edition

# CHAPTER 1 DESCRIPTION

This chapter explains a feature and a basic specification of the MB95130/M series.

- 1.1 Feature of MB95130/M Series
- 1.2 Product Lineup of MB95130/M Series
- 1.3 Difference Points among Products and Notes on Selecting a Product
- 1.4 Block Diagram of MB95130/M Series
- 1.5 Pin Assignment
- 1.6 Package Dimension
- 1.7 Pin Description
- 1.8 I/O Circuit Type

### 1.1 Feature of MB95130/M Series

# In addition to a compact instruction set, the MB95130/M series is a general-purpose single-chip microcontroller built-in abundant peripheral functions.

#### ■ Feature of MB95130/M Series

• F<sup>2</sup>MC-8FX CPU core

Instruction system optimized for controllers

- Multiplication and division instructions
- 16-bit operation
- Bit test branch instruction
- Bit operation instructions, etc.

#### Clock

- Main clock
- Main PLL clock
- Sub clock (Only for two-system product)
- Sub PLL clock (Only for two-system product)

#### Timer

- 8/16-bit composite timer
- 8/16-bit PPG
- 16-bit PPG
- Timebase timer
- Watch prescaler (Only for two-system product)

#### LIN-UART

- With full-duplex double buffer
- · An asynchronous clock or a synchronous serial data transfer can be used

#### UART/SIO

- With full-duplex double buffer
- An asynchronous clock or a synchronous serial data transfer can be used
- External interrupt
  - Interrupt by the edge detection (Select from rising edge, falling edge, or both edges)
  - Can be used to recover from low-power consumption (standby) mode
- 8/10-bit A/D converter

8-bit or 10-bit resolutions can be selected

• Low-power consumption (standby) mode

- Stop mode
- Sleep mode
- Watch mode (Only for two-system product)
- Timebase timer
- I/O port: Max 20

General-purpose I/O ports (CMOS) : 20

• Programmable input voltage levels of port

Automotive input level / CMOS input level / hysteresis input level

• Flash memory security function

Protects the content of Flash memory (Flash memory device only)

## 1.2 **Product Lineup of MB95130/M Series**

# MB95130/M series is available in three types. Table 1.2-1 lists the product lineup and Table 1.2-2 lists the CPUs and peripheral functions.

#### ■ Product Lineup of MB95130/M Series

Table 1.2-1 Product Lineup of MB95130/M Series

Classification*1		Product ROM/RAM		Voltago	Option		Pocot output
			voliage	Clock system	LVD	Resei ouipui	
<b>F 1</b>		MD05EV100D 101	60VD/2 75VD	3V	Single system	None	None
		MB95F V 100D-101	00KD/3./3KD		Two-system		
					Single system	None	Vas
Evaluation	products	MB95EV100D-103	60KB/3 75KB	5V	Yes	Yes	165
		WID)51 V 100D-105	00KD/3./3KD	5.	Two system	None	Ves
					Two-system	Yes	103
		MB95F133MS	8KB/256B	5V	Single system	None	Yes
	Flash memory products	MB95F133NS	8KB/256B	5V	Single system	Yes	Yes
		MB95F133MW	8KB/256B	5V	Dual-system	None	Yes
		MB95F133NW	8KB/256B	5V	Dual-system	Yes	Yes
		MB95F134MS	16KB/512B	5V	Single system	None	Yes
		MB95F134NS	16KB/512B	5V	Single system	Yes	Yes
		MB95F134MW	16KB/512B	5V	Dual-system	None	Yes
5V products		MB95F134NW	16KB/512B	5V	Dual-system	Yes	Yes
-		MB95F136MS	32KB/1KB	5V	Single system	None	Yes
		MB95F136NS	32KB/1KB	5V	Single system	Yes	Yes
		MB95F136MW	32KB/1KB	5V	Two-system	None	Yes
		MB95F136NW	32KB/1KB	5V	Two-system	Yes	Yes
		MB95136M			Single system	None	Yes
	Mask ROM		32KB/1KB	5V	Single system	Yes	
	products*3	1.12/010000	5210,110	5,	Two-system	None	Yes
					100 555000	Yes	105

LVD: Low-voltage detection reset

\*1: 3V products are under planning.

\*2: On evaluation products, toggle single/two system and whether to include LVD with the switch on MCU board.

\*3: On mask ROM products, specify single/two system and whether to include LVD when issuing the mask ROM order.

Item		Specification		
CPU function		Number of basic instructions: 136 instructions Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, and 16 bits Minimum instruction execution time: 61.5 ns (at machine clock 16.25 MHz) Interrupt processing time: 0.6 µs (at machine clock 16.25 MHz)		
	Port	General-purpose I/O ports (CMOS): 20 (Max)		
	Timebase timer	Interrupt cycle: 0.5 ms, 2.1 ms, 8.2 ms, 32.8 ms (at external 4 MHz)		
	Watchdog timer	Reset generation cycle         Main clock at 10 MHz       : 105 ms (Min)         Sub clock at 32.768 kHz (Only for two-system product): 250 ms (Min)		
	Wild registers	ROM data for three bytes can be replaced		
	UART/SIO	Data transfer is enabled at UART/SIO Built-in full-duplex double buffer, Changeable data length (5/6/7/8-bit), Built-in baud rate generator NRZ method transfer format, Error detected function LSB-first or MSB-first can be selected Serial data transfer is available for clock synchronous (SIO) and clock asynchronous (UART)		
	LIN-UART	A wide-range communication speed can be set with the dedicated reload timer Full-duplex double buffer Serial data transfer is available for clock synchronous and clock asynchronous LIN function can be used as a LIN master and LIN slave		
	8/10-bit A/D converter	8ch. 8-bit or 10-bit resolution can be selected		
Peripheral	8/16-bit composite timer	Can be configured as a 2ch × 8-bit timer or 1ch × 16-bit timer Built-in timer function, PWC function, PWM function and capture function Count clock: available from internal clocks (7 types) or external clocks With square wave output		
Tunetion	16-bit PPG	PWM mode or one-shot mode can be selected Counter operation clock: Available from eight selectable clock sources Support for external trigger activation		
	8/16-bit PPG	Can be configured as a $2ch \times 8$ -bit PPG or $1ch \times 16$ -bit PPG Counter operation clock: Available from eight selectable clock sources		
	Watch counter	Count clock: Available from four selectable clock sources (125 ms, 250 ms, 500 ms, or 1 s) Counter value can be set within the range of 0 to 63 (When one second is selected as for the clock source and the counter value is set to 60, it is possible to count for one minute.) Note: At selecting the two-system product		
	Watch prescaler	Available from four selectable interval times (125 ms, 250 ms, 500 ms, 1 s) Note: At selecting the two-system product		
	External interrupt	8ch. Interrupt by edge detection (Select from rising edge, falling edge, or both edges) Can be used to recover from standby modes		
	Flash memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of write/erase cycles (Minimum) : 10000 times Data retention time: 20 years Erase can be performed on each block Block protection with external programming voltage Elash Sequeity Feature for protecting the context of the Elash		
Standby Mode		Sleep, stop, watch (Only for two-system product), and timebase timer		

Table 1.2-2 CPU and Peripheral Function of MB95130/M Series

### 1.3 Difference Points among Products and Notes on Selecting a Product

# The following describes differences among MB95130/M series products and notes when selecting the product.

#### ■ Difference Points among Products and Notes on Selecting a Product

- Notes on using evaluation products
  - The evaluation products are intended to support software development for a number of different  $F^2MC-8FX$  family series and products, and it therefore includes additional functions that may not be included in MB95130/M series. Accordingly, access to I/O address of peripheral functions that are not used in MB95130/M series is prohibited.

Reading or writing to these prohibited addresses may cause these unused peripheral functions to operate and lead to unexpected hardware or software problems.

Take particular care not to use word access to read or write odd numbered bytes in the prohibited areas (It causes unexpected read/write operation).

Also, as the read values of prohibited addresses on the evaluation product are different to the values on the flash memory and mask ROM products, do not use these values in the program.

The functions corresponding to certain bits in single-byte registers may not be supported on some mask ROM and flash memory products. However, reading or writing to these bits will not cause malfunction of the hardware. Also, as the evaluation, flash memory, and mask ROM products are designed to have identical software operation, no particular precautions are required.

#### Difference of memory space

If the memory size on the evaluation product is different to the flash memory or mask ROM product, please ensure you understand these differences when developing software.

#### Current consumption

The current consumption of flash memory products is greater than for mask ROM products.

For the details of current consumption, refer to "**E**LECTRICAL CHARACTERISTICS" in data sheet.

#### Package

For detailed information on each package, see "■Package and Its Corresponding Product" and "1.6 Package Dimension".

#### Operating voltage

The operating voltage may be different depending on the products. For the details, see "■ELECTRICAL CHARACTERISTICS" in "data sheet".

#### • Difference of MOD pin

For mask ROM products, a pull-down resistor is provided for the MOD pin.

## Package and Its Corresponding Product

Product Package	MB95136M	MB95F133MS MB95F133NS MB95F133MW MB95F133NW MB95F134MS MB95F134NS MB95F134MW MB95F134NW MB95F136MS MB95F136NS MB95F136NW	MB95FV100D-101 MB95FV100D-103
FPT-28P-M17	О	О	×
BGA-224P-M08	×	X	О

O:usable

 $\times$ : unusable

#### 1.4 **Block Diagram of MB95130/M Series**

#### Figure 1.4-1 shows the block diagram of all MB95130/M series.

#### Block Diagram of All MB95130/M Series





## 1.5 Pin Assignment

#### Figure 1.5-1 shows the pin assignment of the MB95130/M series.

#### ■ Pin Assignment of MB95130/M Series



## 1.6 Package Dimension

#### MB95130/M series is available in 1 type of package.

#### ■ Package Dimension of FPT-28P-M17

28-pin plastic SOP Lead pitch 1.27 mm Package width ×  $8.6 \times 17.75 \text{ mm}$ package length Lead shape Gullwing FREEERE Sealing method Plastic mold Mounting height 2.80 mm MAX Weight 0.82 g Code (FPT-28P-M17) P-SOP28-8.6 × 17.75-1.27 (Reference)

Figure 1.6-1 Package Dimension of FPT-28P-M17



Please confirm the latest Package dimension by following URL. http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

## **1.7 Pin Description**

# Table 1.7-1 shows pin description. The alphabet in the "Circuit Type" column of Table1.7-1 corresponds to the one in the "Classification" column of Table 1.8-1.

### Pin Description

Table 1.7-1	Pin	Description	(1	12)
		Description	• •	, _,

Pin No.	Pin Name	Circuit Type	Function Description	
1	P16	Н	General-purpose I/O port.	
2	PF0	V		
3	PF1	ĸ	General-purpose I/O port.	
4	MOD	В	Operation mode specification pin.	
5	X0	٨	Oscillation pin for the main clock.	
6	X1	А		
7	Vss	-	Power supply (GND) pin.	
8	Vcc	-	Power supply pin.	
9	PG0/C	Н	General-purpose I/O port (at 3 V). Capacitance connection pin (at 5 V).	
10	X1A/PG2	A /TT	Oscillation pin for the sub clock.	
11	X0A/PG1	A/H	(32kHz) Single system product is general-purpose port.	
12	RST	B'	Reset pin.	
13	AVcc	-	Power supply pin for A/D converter.	
14	AVss	-	Power supply (GND) pin for A/D converter.	
15	P00/INT00/ AN00/PPG00	D	General-purpose I/O port. This pin is also used for external interrupt input (INT00), A/D converter analog input (AN00) and 8/16-bit PPG ch.0 output (PPG00).	
16	P01/INT01/ AN01/PPG01		General-purpose I/O port. This pin is also used for external interrupt input (INT01), A/D converter analog input (AN01) and 8/16-bit PPG ch.0 output (PPG01).	
17	P02/INT02/ AN02/SCK		General-purpose I/O port. This pin is also used for external interrupt input (INT02), A/D converter analog input (AN02) and LIN-UART clock I/O (SCK).	
18	P03/INT03/ AN03/SOT		General-purpose I/O port. This pin is also used for external interrupt input (INT03), A/D converter analog input (AN03) and LIN-UART data output (SOT).	
19	P04/INT04/ AN04/SIN	Е	General-purpose I/O port. This pin is also used for external interrupt input (INT04), A/D analog input (AN04) and LIN-UART data input (SIN).	

#### Table 1.7-1 Pin Description (2 / 2)

Pin No.	Pin Name	Circuit Type	Function Description
20	P05/INT05/ AN05/TO00		General-purpose I/O port. These pins are also used for external interrupt input (INT05,INT06),
21	P06/INT06/ AN06/TO01	D	A/D converter analog input (AN05,AN06) and 8/16-bit composite timer ch.0 output (TO00, TO01).
22	P07/INT07/ AN07		General-purpose I/O port. This pin is also used for external interrupt input (INT07), A/D converter analog input (AN07).
23	P10/UI0	G	General-purpose I/O port. This pin is also used for UART/SIO ch.0 data input.
24	P11/UO0		General-purpose I/O port. This pin is also used for UART/SIO ch.0 data output.
25	P12/UCK0/EC0		General-purpose I/O port. This pin is also used for UART/SIO ch.0 clock I/O (UCK0) and 8/16-bit composite timer ch.0 clock input (EC0).
26	P13/TRG0/ ADTG	Н	General-purpose I/O port. This pin is also used for 16-bit PPG ch.0 trigger input (TRG0) and A/D converter trigger input (ADTG).
27	P14/PPG0		General-purpose I/O port. This pin is also used for 16-bit PPG ch.0 output.
28	P15		General-purpose I/O port.

## 1.8 I/O Circuit Type

Table 1.8-1 lists the I/O circuit types. Also, the alphabet in the "Classification" column of Table 1.8-1 corresponds to the one in the "Circuit Type" column of Table 1.7-1.

#### ■ I/O Circuit Type

#### Table 1.8-1 I/O Circuit Type (1 / 2)

Туре	Circuit	Remarks
A	X1 (X1A) X0 (X0A) Standby control	<ul> <li>Oscillation circuit</li> <li>High-speed side Feedback resistance: approx. 1 MΩ</li> <li>Low-speed side Feedback resistance: approx. 10 MΩ</li> </ul>
В	R R H	• Only for input Hysteresis input only for MASK ROM product Pull-down resistor available only to MASK ROM product
B'	Reset input	<ul> <li>Hysteresis input only for MASK ROM product</li> <li>Reset output</li> </ul>
D	A/D control	<ul> <li>CMOS output</li> <li>Hysteresis input</li> <li>Analog input</li> <li>Pull-up control available</li> <li>Automotive input</li> </ul>

#### Table 1.8-1 I/O Circuit Type (2 / 2)



# CHAPTER 2 HANDLING DEVICES

This chapter gives notes on using.

2.1 Device Handling Precautions

### 2.1 Device Handling Precautions

# This section summarizes the precautions on the device's power supply voltage and pin treatment.

#### Device Handling Precautions

#### Preventing Latch-up

Care must be taken to ensure that maximum voltage ratings are not exceeded when they are used.

Latch-up may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between  $V_{CC}$  pin and  $V_{SS}$  pin.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage  $(AV_{CC})$  and analog input voltage from exceeding the digital power supply voltage  $(V_{CC})$  when the analog system power supply is turned on or off.

#### Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the Vcc power-supply voltage.

For stabilization, in principle, keep the variation in Vcc ripple (p-p value) in a commercial frequency range (50 Hz/60 Hz) not to exceed 10% of the standard Vcc value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

#### Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub clock mode or stop mode.

#### Precautions for Debug

When using an evaluation device (mounted on an MCU board) for software development, there may be some differences between the operation of the evaluation device and the device you will actually use. The following lists some points to note during development.

#### SYCC Register Settings

During debugging, the values of the DIV1 and DIV0 bits in the SYCC register may differ from the user settings. This is because, when a break occurs, the CPU adjusts the communications speed between the evaluation device and the BGM adapter to use the optimum speed.

To prevent this from occurring, you need to set response speed optimization to disabled.

This point is explained in "Section 2.3.1 of the Function Description for the SOFTUNE WORKBENCH development environment". Please refer to this document also.

#### Flash Memory Types and Sizes

Each evaluation device can be used for debugging of a number of different production models (series). When developing your program, please take note of the actual ROM and RAM sizes on the device you intend to use.

Further, evaluation devices use dual-operation flash memory. However, some production models have flash memory containing only one sector. Please take note of any differences between the flash memory configurations of the production and evaluation devices, particularly if writing a program that performs self-updating of flash memory.

#### Differences in Flash Memory Content

The debugger for the  $F^2MC-8FX$  family uses the software break instruction to implement break points. When continuous or step execution is performed after setting a break point, the software break instruction is written to the break address in the flash memory on the evaluation device.

Accordingly, the contents of flash memory after a software break has been inserted by the debugger will be different to the program data image generated by the compiler. Before performing a checksum, you must remember to clear all break points and "synchronize flash memory".

Restrictions Relating to the Flash Memory on the Evaluation Device

The following restrictions apply to the evaluation device for the  $F^2MC-8FX$  family.

- (1) Writing or erasing the lower bank (addresses 1000H-3FFFH) is not possible. When debugging, please do this on the production flash memory model.
- (2) Do not use the chip erase command for the flash memory on the evaluation device. When debugging, please do this on the production flash memory model.

#### Operation of Peripheral Functions During a Break

When a CPU break occurs, the debugger for the  $F^2MC-8FX$  family halts CPU operation (instruction code fetch, decoding, instruction execution, updating the PC, etc.) but the peripheral functions (PPG timer, UART, A/D converter, etc.) continue to operate.

The following are some example implications:

- (1) If the overflow flag for a timer/counter is set during a CPU break and the interrupt is enabled, the interrupt routine will run immediately when execution restarts after the break.
- (2) Clearing the overflow flag for a timer/counter via the memory window or similar during a CPU break will not appear to work as the flag will quickly be reset again.

#### Prohibited Access to Undefined I/O Addresses

The debugger for the  $F^2MC$ -8FX family uses the same evaluation device for debugging all models. This evaluation device includes all peripheral functions that may be used during debugging. Accessing a register that does not exist on your target production device may invoke a peripheral function that should not exist and may result in abnormal operation. Accordingly, please do not access undefined address areas.

#### Pin Connection

Treatment of Unused Pin

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leaving to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k $\Omega$ . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins. If there is unused output pin, make it open.

• Treatment of Power Supply Pins on A/D Converter

Connect to be  $AV_{CC} = V_{CC}$  and  $AV_{SS} = V_{SS}$  even if the A/D converter is not in use.

Noise riding on the AV<sub>CC</sub> pin may cause accuracy degradation. So, connect approx. 0.1  $\mu$ F ceramic capacitor as a bypass capacitor between AV<sub>CC</sub> and AV<sub>SS</sub> pins in the vicinity of this device.

#### Power Supply Pins

In products with multiple  $V_{CC}$  or  $V_{SS}$  pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the  $V_{CC}$  and  $V_{SS}$  pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1  $\mu$ F between V<sub>CC</sub> and V<sub>SS</sub> pins near this device.

#### Mode Pin (MOD)

Connect the mode pin directly to V<sub>CC</sub> or V<sub>SS</sub>.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  and to provide a low-impedance connection.

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. A bypass capacitor of  $V_{CC}$  pin must have a capacitance value higher than  $C_S$ . For connection of smoothing capacitor  $C_S$ , see the diagram below.



Figure 2.1-1 C pin connection diagram

#### NC Pins

Any pins marked "NC" (not connected) must be left open.

#### • Analog Power Supply

Always set the same potential to  $AV_{CC}$  and  $V_{CC}$ . When  $V_{CC} > AV_{CC}$ , the current may flow through the AN00 to AN07 pins.

#### CHAPTER 2 HANDLING DEVICES
# CHAPTER 3 MEMORY SPACE

This chapter describes memory space.

- 3.1 Memory Space
- 3.2 Memory Map

# 3.1 Memory Space

The memory space on the F<sup>2</sup>MC-8FX family is 64 K bytes, divided into I/O, extended I/O, data, and program areas. The memory space includes special-purpose areas such as the general-purpose registers and vector table.

#### Configuration of Memory Space

- I/O area (addresses: 0000<sub>H</sub> to 007F<sub>H</sub>)
  - This area contains the control registers and data registers for on-chip peripheral resources.
  - As the I/O area is allocated as part of memory space, it can be accessed in the same way as for memory. It can also be accessed at higher speed by using direct addressing instructions.
- Extended I/O area (addresses: 0F80<sub>H</sub> to 0FFF<sub>H</sub>)
  - This area contains the control registers and data registers for on-chip peripheral resources.
  - As the extended I/O area is allocated as part of memory space, it can be accessed in the same way as for memory.
- Data area
  - Static RAM is incorporated as the internal data area.
  - The internal RAM capacity is different depending on the product.
  - The RAM area from  $80_{\rm H}$  to  ${\rm FF}_{\rm H}$  can be accessed at higher speed by using direct addressing instructions.
  - The area from  $100_{\rm H}$  to  $47F_{\rm H}$  is an extended direct addressing area. It can be accessed at higher speed by direct addressing instructions with the direct bank pointer set.
  - Addresses  $100_{\rm H}$  to  $1FF_{\rm H}$  can be used as a general-purpose register area.

#### Program area

- ROM is incorporated as the internal program area.
- The internal ROM capacity is different depending on the model.
- Addresses  $FFC0_H$  to  $FFFF_H$  are used as the vector table.

#### Memory Map



Figure 3.1-1 Memory Map

## 3.1.1 Areas for Specific Applications

# The general-purpose register area and vector table area are used for the specific applications.

#### ■ General-purpose Register Area (Addresses: 0100<sub>H</sub> to 01FF<sub>H</sub>)

- This area contains the auxiliary registers used for 8-bit arithmetic or transfer operations.
- As the area is allocated as part of the RAM area, it can also be used as ordinary RAM.
- When the area is used as general-purpose registers, general-purpose register addressing enables higherspeed access using short instructions.

For details, see Section "5.1.1 Register Bank Pointer (RP)" and Section "5.2 General-purpose Registers".

#### ■ Vector Table Area (Addresses: FFC0<sub>H</sub> to FFF<sub>H</sub>)

- This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
- The vector table area is allocated at the top of the ROM area. At the individual addresses in the vector table, the start addresses of their respective service routines are set as data.

Table 8.1-1 lists the vector table addresses to be referenced for vector call instructions, interrupts, and for resets.

For details, see CHAPTER 8 INTERRUPTS, CHAPTER 7 RESET, and "● CALLV #vct" in Appendix E.2 "Special Instructions".

### 3.2 Memory Map

This section gives a memory map of the MB95130/M series.

#### Memory Map



25

	Flash memory	RAM	Address #1	Address #2	
MB95F133MS/F133NS	8 Khytas	256 bytes	0180	E000	
MB95F133MW/F133NW	8 KUyles	250 bytes	0180 <sub>H</sub>	E000H	
MB95F134MS/F134NS	16 Vbutas	512 hyter	0380	C000	
MB95F134MW/F134NW	10 KDytes	512 bytes	0280 <sub>H</sub>	$C000_{\rm H}$	
MB95F136MS/F136NS	20 Khutaa	1 Khutaa	0.480	8000	
MB95F136MW/F136NW	52 KDytes	1 Köytes	0480 <sub>H</sub>	8000 <sub>H</sub>	

# CHAPTER 4 MEMORY ACCESS MODE

This chapter describes the memory access mode.

4.1 Memory Access Mode

### 4.1 Memory Access Mode

# The memory access mode supported by the MB95130/M series is only single-chip mode.

#### ■ Single-chip Mode

Single-chip mode uses only internal RAM and ROM without using an external bus access.

#### Mode data

Mode data is used to determine the memory access mode of the CPU.

The mode data address is fixed as  $FFFD_H$  (The value of  $FFFC_H$  can be any value). Be sure to set the mode data of internal ROM to "00<sub>H</sub>" to select single-chip mode.

Figure 4.1-1 Mode Data Settings



After a reset, the CPU fetches mode data first.

The CPU then fetches the reset vector after the mode data. The instruction is performed from the address set by reset vector.

#### Mode pin (MOD)

Be sure to set the mode pin (MOD) to  $V_{SS}$ .

# CHAPTER 5 CPU

This chapter describes functions and operations of the CPU.

- 5.1 Dedicated Registers
- 5.2 General-purpose Registers
- 5.3 Placement of 16-bit Data in Memory

# 5.1 Dedicated Registers

The CPU has its dedicated registers: the program counter (PC), two arithmetic registers (A and T), three address pointers (IX, EP, and SP), and the program status (PS) register. Each of the registers is 16 bits long. The PS register consists of the register bank pointer (RP), direct pointer (DP), and condition code register (CCR).

#### Configuration of Dedicated Registers

The dedicated registers in the CPU are seven 16-bit registers. Accumulator (A) and temporary accumulator (T) can also be used with only their lower eight bits in service.

Figure 5.1-1 shows the configuration of the dedicated registers.

	Figu	re 5.1-1 CO	iniguration of Deulcaleu Registers
Initial value	16 k	oits	
FFFD <sub>H</sub>	PC	2	- : Program counter
			Contains the address of the current instruction.
0000 <sub>H</sub>	AH	AL	: Accumulator (A)
	I		Temporary storage register for arithmetic operation and transfer.
0000 <sub>H</sub>	ТН	TL	: Temporary accumulator (T)
			Performs an operation with accumulator.
0000 <sub>H</sub>	IX	(	: Index register
			Register containing an index address.
0000 <sub>H</sub>	EF	5	: Extra pointer
			Pointer containing a memory address.
0000 <sub>H</sub>	SF	5	: Stack pointer
			Contains the current stack location.
0030 <sub>H</sub>	RP DP	CCR	: Program status
	P	S	Register consisting of the register bank pointer, direct bank pointer, and condition code register.

#### gure 5.1-1 Configuration of Dedicated Registers

#### Functions of Dedicated Registers

Program counter (PC)

The program counter is a 16-bit counter which contains the memory address of the instruction currently executed by the CPU. The program counter is updated whenever an instruction is executed or an interrupt or reset occurs. The initial value set immediately after a reset is the mode data read address ( $FFFD_H$ ).

• Accumulator (A)

The accumulator is a 16-bit register for arithmetic operation. It is used for a variety of arithmetic and transfer operations of data in memory or data in other registers such as the temporary accumulator (T). The data in the accumulator can be handled either as word (16-bit) data or byte (8-bit) data. For byte-length arithmetic and transfer operations, only the lower eight bits (AL) of the accumulator are used with the upper eight bits (AH) left unchanged. The initial value set immediately after a reset is " $0000_{\rm H}$ ".

#### Temporary accumulator (T)

The temporary accumulator is an auxiliary 16-bit register for arithmetic operation. It is used to perform arithmetic operations with the data in the accumulator (A). The data in the temporary accumulator is handled as word data for word-length (16-bit) operations with the accumulator (A) and as byte data for byte-length (8-bit) operations. For byte-length operations, only the lower eight bits (TL) of the temporary accumulator are used and the upper eight bits (TH) are not used.

When a MOV instruction is used to transfer data to the accumulator (A), the previous contents of the accumulator are automatically transferred to the temporary accumulator. When transferring byte-length data, the upper eight bits (TH) of the temporary accumulator remain unchanged. The initial value after a reset is " $0000_{\text{H}}$ ".

#### Index register (IX)

The index register is a 16-bit register used to hold the index address. The index register is used with a single-byte offset (-128 to +127). The offset value is added to the index address to generate the memory address for data access. The initial value after a reset is " $0000_{\rm H}$ ".

#### Extra pointer (EP)

The extra pointer is a 16-bit register which contains the value indicating the memory address for data access. The initial value after a reset is " $0000_{\text{H}}$ ".

#### Stack pointer (SP)

The stack pointer is a 16-bit register which holds the address referenced when an interrupt or subroutine call occurs and by the stack push and pop instructions. During program execution, the value of the stack pointer indicates the address of the most recent data pushed onto the stack. The initial value after a reset is " $0000_{\text{H}}$ ".

#### Program status (PS)

The program status is a 16-bit control register. The upper eight bits make up the register bank pointer (RP) and direct bank pointer (DP); the lower eight bits make up the condition code register (CCR).

In the upper eight bits, the upper five bits make up the register bank pointer used to contain the address of the general-purpose register bank. The lower three bits make up the direct bank pointer which locates the area to be accessed at high speed by direct addressing.

The lower eight bits make up the condition code register (CCR) which consists of flags that represent the state of the CPU.

The instructions that can access the program status are MOVW A,PS or MOVW PS,A. The register bank pointer (RP) and direct bank pointer (DP) in the program status register can also be read from or written to by accessing the mirror address (0078<sub>H</sub>).

Note that the condition code register (CCR) is part of the program status register and cannot be accessed independently.

Refer to the "F<sup>2</sup>MC-8FX Programming Manual" for details on using the dedicated registers.

# 5.1.1 Register Bank Pointer (RP)

The register bank pointer (RP) in bits 15 to 11 of the program status (PS) register contains the address of the general-purpose register bank that is currently in use and is translated into a real address when general-purpose register addressing is used.

#### Configuration of Register Bank Pointer (RP)

Figure 5.1-2 shows the configuration of the register bank pointer.

Figure 5.1-2 Configuration of Register Bank Pointer																	
RP DP									CCR								
	/ bit15	bit14	bit13	bit12	bit11	/ bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	RP Initial value
PS	R4	R3	R2	R1	R0	DP2	DP1	DP0	Н	I	IL1	IL0	Ν	Z	V	С	00000 <sub>B</sub>

The register bank pointer contains the address of the register bank currently being used. The content of the register bank pointer is translated into a real address according to the rule shown in Figure 5.1-3.

Figure 5.1-3	Rule for	Translation	into Rea	Addresses i	n General-	purpo	se Rec	lister .	Area
		manolation				P 41 P 4		,	

	Fixed value								RP: Upper					Op-code: Lower			
	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"1"	R4	R3	R2	R1	R0	b2	b1	b0	
	$\downarrow$	↓	₽	↓	₽	$\downarrow$	$\downarrow$	₽	↓	↓	₽	↓	↓	÷	↓	Ŧ	
Generated	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
audi 633																	

The register bank pointer specifies the register bank used as general-purpose registers in the RAM area. There are a total of 32 register banks. The current register bank is specified by setting a value between 0 and 31 in the upper five bits of the register bank pointer. Each register bank has eight 8-bit general-purpose registers which are selected by the lower three bits of the op-code.

The register bank pointer allows the space from " $0100_{\text{H}}$ " to up to " $01\text{FF}_{\text{H}}$  (Max.)" to be used as a generalpurpose register area. Note, however, that the available area is limited depending on the product. The initial value after a reset is " $0000_{\text{H}}$ ".

#### Mirror Address for Register Bank and Direct Bank Pointers

The register bank pointer (RP) and direct bank pointer (DP) can be written to and read from by accessing the program status (PS) register using the "MOVW A,PS" and "MOVW PS,A" instructions, respectively. They can also be written to and read from directly by accessing mirror address " $0078_{\rm H}$ " of the register bank pointer.

## 5.1.2 Direct Bank Pointer (DP)

# The direct bank pointer (DP) in bits 10 to 8 of the program status (PS) register specifies the area to be accessed by direct addressing.

#### ■ Configuration of Direct Bank Pointer (DP)

Figure 5.1-4 shows the configuration of the direct bank pointer.

					iigui	0.1	- 00	migu	auto			Bain					
	RP DP								CCR								
	/				/	/		<u></u> ۱.									DP Initial
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	value
PS	R4	R3	R2	R1	R0	DP2	DP1	DP0	Н	Ι	IL1	IL0	Ν	Z	V	С	000 <sub>B</sub>

#### Figure 5.1-4 Configuration of Direct Bank Pointer

The areas from  $0000_{\rm H}$  to  $007F_{\rm H}$  and  $0080_{\rm H}$  to  $047F_{\rm H}$  can be accessed by direct addressing. Access to  $0000_{\rm H}$  to  $007F_{\rm H}$  is specified with an operand regardless of the value in the direct bank pointer. Access to  $0080_{\rm H}$  to  $047F_{\rm H}$  is specified with the value in the value of the direct bank pointer and the operand.

Table 5.1-1 shows the relationship between direct bank pointer (DP) and access area; Table 5.1-2 lists the direct addressing instructions.

#### Table 5.1-1 Direct Access Pointer and Access Area

Direct bank pointer (DP) [2:0]	Operand-specified dir	Access area
$XXX_{B}$ (It does not affect the mapping. )	$0000_{\mathrm{H}}$ to $007\mathrm{F}_{\mathrm{H}}$	$0000_{\rm H}$ to $007F_{\rm H}$
000 <sub>B</sub> (Initial value)		0080 <sub>H</sub> to 00FF <sub>H</sub>
001 <sub>B</sub>		$0100_{\rm H}$ to $017F_{\rm H}$
010 <sub>B</sub>		0180 <sub>H</sub> to 01FF <sub>H</sub>
011 <sub>B</sub>	0080 to 00FF	0200 <sub>H</sub> to 027F <sub>H</sub>
100 <sub>B</sub>	OCCOLT TO COLT H	$0280_{\rm H}$ to $02{\rm FF}_{\rm H}$
101 <sub>B</sub>		$0300_{\mathrm{H}}$ to $037\mathrm{F}_{\mathrm{H}}$
110 <sub>B</sub>		$0380_{\rm H}$ to $03{\rm FF}_{\rm H}$
111 <sub>B</sub>		0400 <sub>H</sub> to 047F <sub>H</sub>

Applicable Instruction
CLRB dir:bit
SETB dir:bit
BBC dir:bit,rel
BBS dir:bit,rel
MOV A,dir
CMP A,dir
ADDC A,dir
SUBC A,dir
MOV dir,A
XOR A,dir
AND A,dir
OR A,dir
MOV dir,#imm
CMP dir,#imm
MOVW A,dir
MOVW dir,A

#### Table 5.1-2 Direct Address Instruction List

# 5.1.3 Condition Code Register (CCR)

The condition code register (CCR) in the lower eight bits of the program status (PS) register consists of the bits (H, N, Z, V, and C) containing information about the arithmetic result or transfer data and the bits (I, IL1, and IL0) used to control the acceptance of interrupt requests.

#### ■ Configuration of Condition Code Register (CCR)

				Fig	jure 5	5.1-5	Conf	igura	tion o	of Cor	nditio	n Coo	de Re	giste	r		
			RP				DP					CC	CR				
	/ bit15	bit14	bit13	bit12	bit11	/ bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	CCR Initial value
PS	R4	R3	R2	R1	R0	DP2	DP1	DP0	Н	I	IL1	IL0	Ν	Z	V	С	00110000 <sub>B</sub>
			Ha Int Ne Ze Ov Ca	If carry errupt of egative ro flag verflow arry flag	flag - enable evel bi flag — flag —	flag — ts —											

The condition code register is a part of the program status (PS) register and therefore cannot be accessed independently.

#### Bits Result Information Bits

• Half carry flag (H)

This flag is set to "1" when a carry from bit 3 to bit 4 or a borrow from bit 4 to bit 3 occurs as the result of an operation. Otherwise, the flag is set to "0". Do not use this flag for any operation other than addition and subtraction as the flag is intended for decimal-adjusted instructions.

Negative flag (N)

This flag is set to "1" when the value of the most significant bit is "1" as the result of an operation and set to "0" if the value is "0".

Zero flag (Z)

This flag is set to "1" when the result of an operation is "0" and set to "0" otherwise.

• Overflow flag (V)

This flag indicates whether an operation has resulted in an overflow, assuming the operand used for the operation as an integer represented by a two's complement. The flag is set to "1" when an overflow occurs and set to "0" otherwise.

#### • Carry flag (C)

This flag is set to "1" when a carry from bit 7 or a borrow to bit 7 occurs as the result of an operation. Otherwise, the flag is set to "0". When a shift instruction is executed, the flag is set to the shift-out value. Figure 5.1-6 shows how the carry flag is updated by a shift instruction.





#### Interrupt Acceptance Control Bits

#### Interrupt enable flag (I)

When this flag is set to "1", interrupts are enabled and accepted by the CPU. When this flag is set to "0", interrupts are disabled and rejected by the CPU.

The initial value after a reset is "0".

The SETI and CLRI instructions set and clear the flag to "1" and "0", respectively.

#### Interrupt level bits (IL1, IL0)

These bits indicate the level of the interrupt currently accepted by the CPU.

The interrupt level is compared with the value of the interrupt level setting register (ILR0 to ILR5) that corresponds to the interrupt request (IRQ0 to IRQ23) of each peripheral resource.

The CPU services an interrupt request only when its interrupt level is smaller than the value of these bits with the interrupt enable flag set (CCR: I = 1). Table 5.1-3 lists interrupt level priorities. The initial value after a reset is " $11_B$ ".

#### Table 5.1-3 Interrupt Levels

IL1	IL0	Interrupt Level	Priority
0	0	0	High
0	1	1	<b>▲</b>
1	0	2	▼
1	1	3	Low (No interrupt)

The interrupt level bits (IL1, IL0) are usually " $11_B$ " with the CPU not servicing an interrupt (with the main program running).

For details on interrupts, see "8.1 Interrupts".

# 5.2 General-purpose Registers

The general-purpose registers are memory blocks consisting of eight 8-bit registers per bank. A total of up to 32 register banks can be used. The register bank pointer (RP) is used to specify the register bank.

Register banks are useful for interrupt handling, vector call processing, and subroutine calls.

#### ■ Configuration of General-purpose Registers

- The general-purpose registers are 8-bit registers and are located in register banks in the general-purpose register area (in RAM).
- Up to 32 banks can be used, where each bank consists of eight registers (R0 to R7).
- The register bank pointer (RP) specifies the register bank currently being used and the lower three bits of the op-code specify general-purpose register 0 (R0) to 7 (R7).

Figure 5.2-1 shows the configuration of the register banks.



Figure 5.2-1 Configuration of Register Banks

For information on the general-purpose register area available on each model, see "3.1.1 Areas for Specific Applications".

#### Features of General-purpose Registers

There are the following features in the general-purpose registers:

- High-speed access to RAM using short instructions (general-purpose register addressing).
- Blocks of register banks facilitating data backup and division by function unit.

General-purpose register banks can be allocated exclusively for specific interrupt service routines or vector call (CALLV #0 to #7) processing routines. An example is always using the fourth register bank for the second interrupt.

Only specifying a dedicated register bank at the beginning of an interrupt service routine automatically saves the general-purpose registers before the interrupt. This eliminates the need for pushing general-purpose register data onto the stack, allowing the CPU to accept interrupts at high speed.

Notes:

- When coding an interrupt service routine, be careful not to change the value of the interrupt level bits (CCR: IL1, IL0) in the condition code register when specifying the register bank by updating the register bank pointer (RP) in that routine. Perform the programming by using either of them.
- Read the interrupt level bits and save their value before writing to the RP.
- Directly write to the RP mirror address "0078<sub>H</sub>" to update the RP.

### 5.3 Placement of 16-bit Data in Memory

#### This section describes how 16-bit data is stored in memory.

#### Placement of 16-bit Data in Memory

State of 16-bit data stored in RAM

When you write 16-bit data to memory, the upper byte of the data is stored at a smaller address and the lower byte is stored at the next address. When you read 16-bit data, it is handled in the same way.

Figure 5.3-1 shows how 16-bit data is placed in memory.



Figure 5.3-1 Placing 16-bit Data in Memory

#### State of operand-specified 16-bit data

In the same way, even when the operands in an instruction specifies 16-bit data, the upper byte is stored at the address closer to the op-code (instruction) and the lower byte is stored at the next address.

That is true whether the operands are either memory addresses or 16-bit immediate data.

Figure 5.3-2 shows how 16-bit data in an instruction is placed.

#### Figure 5.3-2 Storing 16-bit Data in Instruction

[Example]	MOV A, 5678H ; Extended address MOVW A, #1234H ; 16-bit immediate data
	Assemble : XXX0 <sub>H</sub> XX XX XX2 <sub>H</sub> 60 56 78 ; Extended address
	XXX5 <sub>H</sub> E4 12 34 ; 16-bit immediate data XXX8 <sub>H</sub> XX :

State of 16-bit data in the stack

When 16-bit register data is pushed onto the stack upon an interrupt, the upper byte is stored at a lower address in the same way.

CHAPTER 5 CPU

# CHAPTER 6 CLOCK CONTROLLER

This chapter describes the functions and operations of the clock controller.

- 6.1 Overview of Clock Controller
- 6.2 Oscillation Stabilization Wait Time
- 6.3 System Clock Control Register (SYCC)
- 6.4 PLL Control Register (PLLC)
- 6.5 Oscillation Stabilization Wait Time Setting Register (WATR)
- 6.6 Standby Control Register (STBC)
- 6.7 Clock Modes
- 6.8 Operations in Low-power Consumption Modes (Standby Modes)
- 6.9 Clock Oscillator Circuits
- 6.10 Overview of Prescaler
- 6.11 Configuration of Prescaler
- 6.12 Operating Explanation of Prescaler
- 6.13 Notes on Use of Prescaler

### 6.1 Overview of Clock Controller

The F<sup>2</sup>MC-8FX family has a built-in clock controller that optimizes its power consumption. It includes two- system clock product supporting both of the main clock and sub clock and single system clock product supporting only the main clock. The clock controller enables/disables clock oscillation, enables/disables the supply of clock signals to the internal circuitry, selects the clock source, and controls the PLL and frequency divider circuits.

#### Overview of Clock Controller

The clock controller enables/disables clock oscillation, enables/disables clock supply to the internal circuitry, selects the clock source, and controls the PLL and frequency divider circuits.

The clock controller controls the internal clock according to the clock mode, standby mode settings and the reset operation. The current clock mode selects the internal operating clock and the standby mode selects whether to enable or disable clock oscillation and signal supply.

The clock controller selects the optimum power consumption and features depending on the combination of clock mode and standby mode.

Two- system clock product have four different source clocks: a main clock, which is the main oscillation clock divided by two, a sub clock, which is the sub oscillation clock divided by two, a main PLL clock, which is the main oscillation clock multiplied by the PLL multiplier and a sub PLL clock, which is the sub oscillation clock multiplied by the PLL multiplier.

Single system clock product have two different source clocks: a main clock, which is the main oscillation clock divided by two; and a main PLL clock, which is the main oscillation clock multiplied by the PLL multiplier.

#### Block Diagram of the Clock Controller

Figure 6.1-1 shows the block diagram of the clock controller.



Figure 6.1-1 Clock Controller Block Diagram

The clock controller consists of the following blocks:

Main clock oscillator circuit

This block is the oscillator circuit for the main clock.

Sub clock oscillator circuit (Two-system clock product)

This block is the oscillator circuit for the sub clock.

Main PLL oscillator circuit

This block is the oscillator circuit for the main PLL.

Sub PLL oscillator circuit (Two-system clock product)

This block is the oscillator circuit for the sub PLL clock.

System clock selector

This block selects one of the four different source clocks for main clock, sub clock, main PLL clock, and sub PLL clock depending on the clock mode. The prescaler frequency-divides the selected source clock into the machine clock. It is supplied to the clock control circuit.

#### Clock control circuit

This block controls the supply of the machine clock to the CPU and each peripheral resource according to the standby mode or oscillation stabilization wait time.

#### Oscillation stabilization wait circuit

This block outputs the oscillation stabilization wait time signal for each clock from 14 types of main clock oscillation stabilization signals created by the timebase timer and 15 types of sub clock oscillation stabilization signals created by the watch prescaler.

#### System clock control register (SYCC)

This register is used to control current clock mode display, clock mode selection, machine clock divide ratio selection, and sub clock oscillation in main clock mode and main PLL clock mode.

#### Standby control register (STBC)

This register is used to control the transition from RUN state to standby mode, the setting of pin states in stop mode, timebase timer mode, or watch mode, and the generation of software resets.

#### PLL control register (PLLC)

This register is used to enable/disable the oscillation of the main PLL and sub PLL clocks, set the multiplier, and to indicate the stability of PLL oscillation.

#### Oscillation stabilization wait time setting register (WATR)

This register is used to set the oscillation stabilization wait time for the main clock and sub clock.

#### Clock Modes

There are four clock modes available: main clock mode, main PLL clock mode, sub clock mode, and sub PLL clock mode.

Table 6.1-1 shows the relationships between the clock modes and the machine clock (operating clock for the CPU and peripheral resources).

Clock Mode	Machine Clock
Main clock mode	The machine clock is generated from the main clock (main clock divided by 2).
Main PLL clock mode	The machine clock is generated from the main PLL clock (main clock multiplied by the PLL multiplier).
Sub clock mode (Two-system clock product only)	The machine clock is generated from the sub clock (sub clock divided by 2).
Sub PLL clock mode (Two-system clock product only)	The machine clock is generated from the sub PLL clock (sub clock multiplied by the PLL multiplier).

Table 6.1-1 Clock Modes and Machine Clock Selection

In any of the clock modes, the selected clock can also be frequency-divided. Additionally, in modes using a PLL clock, a multiplier for the clock frequency can also be set.

#### Peripheral Resources not Affected by Clock Mode

Note that the peripheral resources listed in the table below are not affected by the clock mode, division, and PLL multiplier settings. Table 6.1-2 lists the peripheral resources not affected by the clock mode.

Table 6.1-2 Peripheral Resources Not Affected by Clock Mode

Peripheral Resource	Operating Clock
Timebase timer	Main clock $(2^{1}/F_{CH})$ : main clock divided by 2)
Watchdog timer	Main clock (with timebase timer output selected) Sub clock (with watch prescaler output selected) (Two-system clock product only)
Watch prescaler (Two-system clock product only)	Sub clock $(2^1/F_{CL}$ : sub clock divided by 2)
Clock counter (Two-system clock product only)	Sub clock (watch prescaler output)

For some peripheral resources other than those listed above, it may be possible to select the timebase timer or watch prescaler output as a count clock. Check the description of each peripheral resource for details.

#### ■ Standby Modes

The clock controller selects whether to enable or disable clock oscillation and clock supply to internal circuitry depending on each standby mode. With the exception of timebase timer mode and watch mode, the standby mode can be set independently of the clock mode.

Table 6.1-3 shows the relationships between standby modes and clock supply states.

Table 6.1-3 Standby Modes and Clock Supply States

Standby Mode	Clock Supply States
Sleep mode	Stops clock supply to the CPU and watchdog timer. As a result, the CPU stops operation, but other peripheral resources continue operating.
Timebase timer mode	Supplies clock signals only to the timebase timer, watch prescaler, and watch counter while stopping clock supply to other circuits. As a result, all the functions other than the timebase timer, watch prescaler, watch counter, external interrupt, and low-voltage detection reset (option) are stopped. Timebase timer mode is only the standby mode for main clock mode or main PLL clock mode.
Watch mode (Two-system clock product only)	Stops main clock oscillation, but supplies clock signals only to the watch prescaler and watch counter while stopping clock supply to other circuits. As a result, all the functions other than the watch prescaler, watch counter, external interrupt, and low-voltage detection reset (option) are stopped. Watch mode is only the standby mode for sub clock mode or sub PLL clock mode.
Stop mode	Stops main clock oscillation and sub clock oscillation and stops the supply of all clock signals. As a result, all the functions other than external interrupt and low-voltage detection reset (option) are stopped.

#### Combinations of Clock Mode and Standby Mode

Table 6.1-4 lists the combinations of clock mode and standby mode and their respective operating states of internal circuits.

Table 6.1-4	Combinations	of Standby	Mode and	Clock Mode	and Internal	Operating	States
-------------	--------------	------------	----------	------------	--------------	-----------	--------

		RI	JN			Sleep				Timebase Timer		Watch (Two- system clock product)		Stop	
Function	Main clock mode	Main PLL clock mode	Sub- clock mode (Two- system clock product)	Sub PLL clock mode (Two- system clock product)	Main clock mode	Main PLL clock mode	Sub- clock mode (Two- system clock product)	Sub PLL clock mode (Two- system clock product)	Main clock mode	Main PLL clock mode	Sub- clock mode (Two- system clock product)	Sub PLL clock mode (Two- system clock product)	Main (PLL) clock mode	Sub PLL clock mode (Two- system clock product)	
Main clock	Oper	ating	Stop	oped	Oper	ating	Stop	oped	Oper	ating	Stop	oped	Stopped	Stopped	
Main PLL clock	Stopped *1	Operat- ing	Stop	oped	Stopped *1	Operat- ing	Stop	oped	Stop	ped*1	Stop	oped	Stopped	Stopped	
Sub clock	Opera	ting <sup>*2</sup>	Oper	Operating		Operating <sup>*2</sup>		erating Operating <sup>*2</sup>		ting <sup>*2</sup>	Operating		Operat- ing <sup>*2</sup>	Stopped	
Sub PLL clock	Stopp	ped*3	Stopped *3	Operat- ing	Stop	ped <sup>*3</sup>	Stopped *3	Operat- ing	Stop	ped <sup>*3</sup>	Stopped *3	Operat- ing	Stopped *3	Stopped	
CPU	Oper	ating	Oper	ating	Stop	ped	Stop	oped	Stopped		Stop	oped	Stopped	Stopped	
ROM RAM	Oper	ating	ng Operating		Value held		Value	e held	Value	e held	Value	e held	Value held	Value held	
I/O ports	Oper	ating	Operating		Outpu	it held	Outpu	it held	Outpu	it held	Outpu	it held	Output held/ Hi-Z	Output held/Hi- Z	
Timebase timer	Oper	ating	Stop	oped	Operating		Stopped		Operating		Stopped		Stopped	Stopped	
Watch prescaler	Opera	ting*2	Oper	ating	Operating <sup>*2</sup>		Operating		Operating <sup>*2</sup>		Operating		Operat- ing <sup>*2</sup>	Stopped	
Watch counter	Opera	ting*2	Oper	ating	Operating <sup>*2</sup>		Operating		Operating <sup>*2</sup>		Oper	ating	Operat- ing <sup>*4</sup>	Stopped	
External interrupt	Oper	ating	Oper	ating	Oper	ating	Oper	ating	Operating		Oper	ating	Operat- ing	Operat- ing	
Watchdog timer	Oper	ating	Oper	ating	Stop	oped	Stop	oped	Stop	oped	Stop	oped	Stopped	Stopped	
Low-voltage detection reset	Oper	ating	Oper	ating	Oper	ating	Oper	ating	Oper	ating	Oper	ating	Operat- ing	Operat- ing	
Other peripheral resources	Oper	ating	Oper	ating	Oper	ating	Oper	ating	Stop	oped	Stop	oped	Stopped	Stopped	

\*1: Operates when the main PLL clock oscillation enable bit in the PLL control register (PLLC:MPEN) is set to "1".

- \*2: Stops when the sub clock oscillation stop bit in the system clock control register (SYCC:SUBS) is set to "1".
- \*3: Operates when the sub PLL clock oscillation enable bit in the PLL control register (PLLC:SPEN) is set to "1".
- \*4: Watch counter keeps counting and no interrupts occur. When the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS) is set to "1", watch counter stops.

## 6.2 Oscillation Stabilization Wait Time

The oscillation stabilization wait time is the time after the oscillator circuit stops oscillation until the oscillator resumes its stable oscillation at its natural frequency. The clock controller obtains the oscillation stabilization wait time by counting a set number of oscillation clock cycles to prevent clock supply to internal circuits.

#### Oscillation Stabilization Wait Time

The clock controller obtains the oscillation stabilization wait time followed by the initiation of oscillation by counting a set number of oscillation clock cycles to prevent clock supply to internal circuits.

When a state transition request for starting oscillation when the power is turned on or for restarting halted oscillation at a clock mode change by a reset, an interrupt in standby mode, or by software, the clock controller automatically waits until the oscillation stabilization wait time for the main clock or sub clock has passed and then causes transition to the next state.

Figure 6.2-1 shows oscillation immediately after being started.



#### Figure 6.2-1 Behavior of Oscillator Immediately after Starting Oscillation

The main clock oscillation stabilization wait time is counted by using the timebase timer. The sub clock oscillation stabilization wait time is counted by using the watch prescaler. The count can be set in the oscillation stabilization wait time setting register (WATR). Set it in keeping with the oscillator characteristics.

When a power-on reset occurs, the oscillation stabilization wait time is fixed to the initial value. For masked ROM products, however, you can specify the initial value of the oscillation stabilization wait time when ordering masked ROM.

Table 6.2-1 shows the length of oscillation stabilization wait time.

Table 6.2-1 Oscillation Stabilization Wait Time

Clock	Factor	Oscillation Stabilization Wait Time
Main clock	Power-on reset	Initial value: $(2^{14}-2)/F_{CH}$ , where $F_{CH}$ is the main clock frequency (specified when ROM is ordered for mask ROM products)
	Other than power-on reset	Register setting value (WATR:MWT3, MWT2, MWT1, MWT0)
Sub clock	Power-on reset	Initial value: $(2^{15}-2)/F_{CL}$ , where $F_{CL}$ is the sub clock frequency.
(Two-system clock product)	Other than power-on reset	Register setting value (WATR:SWT3, SWT2, SWT1, SWT0)

After the oscillation stabilization wait time of the main clock ends, the oscillation stabilization wait time of sub clock measurement is begun.

#### PLL Clock Oscillation Stabilization Wait Time

As with the oscillation stabilization wait time of the oscillator, the clock controller automatically waits for the PLL oscillation stabilization wait time to elapse after a request for state transition from PLL oscillation stopped state to oscillation start is generated via an interrupt in standby mode or a change of clock mode by software.

Note that the PLL clock oscillation stabilization wait time changes according to the PLL startup timing. Table 6.2-2 shows the PLL oscillation stabilization wait time.

Table 6.2-2 PLL Oscillation Stabilization Wait Time

	PLL Oscillation Sta	bilization Wait Time	Remarks		
	Minimum time Maximum tim				
Main PLL clock	$2^{11}/F_{CH} \times 2$	$2^{11}/F_{CH} \times 3$	<ul> <li>Oscillation stabilization wait time is taken while 2<sup>11</sup>/F<sub>CH</sub> is counted twice (minimum) or three times (maximum).</li> <li>F<sub>CH</sub> represents the main clock frequency.</li> </ul>		
Sub PLL clock (Two-system clock product)	$2^{8}/F_{CL} \times 2$	$2^{8}/F_{CL} \times 3$	<ul> <li>Oscillation stabilization wait time is taken while 2<sup>8</sup>/F<sub>CL</sub> is counted twice (minimum) or three times (maximum).</li> <li>F<sub>CL</sub> represents the sub clock frequency.</li> </ul>		

#### Oscillation Stabilization Wait Time and Clock Mode/Standby Mode Transition

The clock controller automatically waits for the oscillation stabilization wait time to elapse as needed when the operating state causes a transition. Depending on the state transition, however, the clock controller does not always wait for the oscillation stabilization wait time.

For details on state transitions, see "6.7 Clock Modes" and "6.8 Operations in Low-power Consumption Modes (Standby Modes)".

#### 6.3 System Clock Control Register (SYCC)

The system clock control register (SYCC) is used to indicate and switch the current clock mode, select the machine clock divide ratio, and control sub clock oscillation in main clock mode and main PLL clock mode.

#### ■ Configuration of System Clock Control Register (SYCC)

Address	bit7	bit6	bit5	bit4	bit3 bi	t2 bit1	bit0 Initial value
0007H	SCM1	SCM0	SCS1	SCS0	SRDY SI	UBS DIV1	DIV0 1010x011 <sub>B</sub>
	R/WX	R/WX	R/W	R/W	R/WX F	R/W R/W	R/W
					<b>D</b> 11/0		
					DIVO	Machine cloc	k divide ratio selection bits
				0	0	Source cloc	К
				0	1	Source cloc	ж / 4
				1	0	Source cloc	ж / 8
				1	1	Source cloc	Ж /16
						Out als als as	- Madan at an Ist
				SOB2	01 1	SUDCIOCK OSC	ciliation stop bit
				0	Starts s		ation
				1	Stops st	UDCIOCK OSCIIIA	ation
				SRDY		Subclock os	cillation stability bit
				0	Indicates wait state	s the subclock e or subclock o	oscillation stabilization oscillation being stopped
				1	Indicate	s subclock os	cillation being stable
				SCS1	SCS0	Cock n	node selection bits
				0	0	Subclock m	ode
				0	1	Sub PLL clo	ock mode
				1	0	Main clock	mode
				1	1	Main PLL c	lock mode
				SCM1	SCM0	Clock m	ode monitor bits
				0	0	Subclock m	ode
				0	1	Sub PLL clo	ock mode
				1	0	Main clock	mode
				1 .	1		a al constanta

Figure 6.3-1 Configuration of System Clock Control Register (SYCC)

: Indeterminate

: Initial value

	Bit name	Function									
bit7 bit6	SCM1, SCM0: Clock mode monitor bits	ndicate the current clock mode. When set to "00 <sub>B</sub> ": the bits indicate sub clock mode. When set to "01 <sub>B</sub> ": the bit indicate sub PLL clock mode. When set to "10 <sub>B</sub> ": the bit indicate main clock mode. When set to "11 <sub>B</sub> ": the bit indicate main PLL clock mode. These bits are read-only: any value attempted to be written is meaningless.									
bit5 bit4	SCS1, SCS0: Clock mode selection bits	pecify the clock mode. <b>When set to "<math>00_B</math>":</b> the bits specify transition to sub clock mode.(Two-system clock product only) <b>When set to "<math>01_B</math>":</b> the bits specify transition to sub PLL clock mode.(Two-system clock product on <b>When set to "<math>10_B</math>":</b> the bits specify transition to main clock mode. <b>When set to "<math>11_B</math>":</b> the bits specify transition to main PLL clock mode. <b>Once a clock mode has been selected in the SCS1 and SCS0 bits, any attempt to write to them is igno until the transition to that clock mode is completed. On single system clock product, an attempt to write "<math>00_B</math>" or "<math>01_B</math>" to these bits is ignored, leaving the value unchanged.</b>									
bit3	SRDY: Sub clock oscillation stability bit (Two-system clock product only)	<ul> <li>Indicates whether sub clock oscillation has become stable.</li> <li>When set to "1", the SRDY bit indicates that the oscillation stabilization wait time for the sub clock has passed.</li> <li>When set to "0", the SRDY bit indicates that the clock controller is in the sub clock oscillation stabilization wait state or that sub clock oscillation has been stopped.</li> <li>This bit is read-only; any value attempted to be written is meaningless.</li> <li>On single system clock product the value of the bit is meaningless.</li> </ul>									
bit2	SUBS: Sub clock oscillation stop bit (Two-system clock product only)	<ul> <li>Stops sub clock oscillation in main clock mode or main PLL clock mode.</li> <li>When set to "0": the bit enables sub clock oscillation.</li> <li>When set to "1": the bit stops sub clock oscillation.</li> <li>Notes:</li> <li>In sub clock mode or sub PLL clock mode, the sub clock oscillates regardless of the value of this bit, except in stop mode.</li> <li>In main clock mode or main PLL clock mode as well, the sub clock oscillates regardless of the value of this bit when sub PLL clock oscillation has been enabled by the PLL clock oscillation enable bit in the PLL control register (PLLC:SPEN).</li> <li>Do not update the SYCC: SCS1 bit and this bit at the same time.</li> </ul>									
bit1 bit0	DIV1, DIV0: Machine clock divide ratio selection bits	<ul> <li>These bits select the machine clock divide ratio to the source clock.</li> <li>The machine clock is generated from the source clock according to the divide ratio set by the bits.</li> <li>DIV1 DIV0 Machine Clock Divide Ratio Selection Bits</li> <li>0 0 Source clock (No division) Main clock divided by 2</li> <li>0 1 Source clock/4 Main clock divided by 8</li> <li>1 0 Source clock/8 Main clock divided by 16</li> <li>1 1 Source clock/16 Main clock divided by 32</li> </ul>									

 Table 6.3-1
 Functions of Bits in System Clock Control Register (SYCC)

# 6.4 PLL Control Register (PLLC)

#### The PLL control register (PLLC) controls the main PLL clock and sub PLL clock.

#### ■ Configuration of PLL Control Register (PLLC)



	Bit name	Function									
bit7	MPEN: Main PLL clock oscillation enable bit	Er me W W In	Enables or disables the oscillation of the main PLL clock in main clock mode or timebase timer mode. When set to "0": the bit disables main PLL clock oscillation. When set to "1": the bit enables main PLL clock oscillation. In main PLL clock mode, the main PLL clock oscillates regardless of the value of this bit either in the RUN state or in sleep mode.								
		Se	t the multiplie	er for the main	PLL clock.						
			MPMC1	MPMC0	Main PLL clock multiplier setting bits	]					
			0	0	Main clock x 1	]					
			0	1	Main clock x 2	]					
bit6	MPMC1, MPMC0:		1	0	Main clock x 2.5	1					
bit5	Main PLL clock		1	1	Setting prohibited	]					
	indupiler setting ons	No	Note: The value of these bits can be changed only when the main PLL clock is stopped. Therefore, do not attempt to update the bits with the PLL clock oscillation enable bit (MPEN) is set to "1" or with the clock mode selection bits in the system clock control register (SYCC: SCS1, SCS0) are set to "11 <sub>B</sub> ". (It is however possible to set these bits at the same time as setting MPEN to "1".)								
bit4	MPRDY: Main PLL clock oscillation stability bit	In In In In In In In In In In	dicates wheth When set to " PLL clock has When set to ' oscillation stal his bit is read-o peration.	er main PLL c 1", the MPRD 5 passed. '0", the MPR bilization wait polly; any value	lock oscillation has become stable. Y bit indicates that the oscillation stabilization DY bit indicates that the clock controller is state or that main PLL clock oscillation has be e attempted to be written is meaningless and h	n wait time for the main in the main PLL clock een stopped. as no effect on the					
bit3	SPEN: Sub PLL clock oscillation enable bit (Two-system clock product only)	Er su W In wa Ev va Or	ables or disables or disables or disable b clock mode, <b>hen set to ''0</b> <b>hen set to ''1</b> sub PLL cloc atch mode. ven in sub PLI lue of this bit. a single syster	les the oscilla or in watch n ": the bit disal ": the bit enab k mode, the su clock mode, n clock produc	tion of the sub PLL clock in main clock mode, node. bles sub PLL clock oscillation. les sub PLL clock oscillation. b PLL clock oscillates regardless of the value the sub PLL clock stops oscillation in stop mo ct, the value of the bit has no effect on the open	main PLL clock mode, of this bit except in ode regardless of the ration.					

 Table 6.4-1
 Functions of Bits in PLL Control Register (PLLC) (1 / 2)

	Bit name	Function								
		Se	Set the multiplier for the Sub PLL clock.							
			SPMC1	SPMC0	Sub PLL Clock Multiplier Setting Bits					
			0 0 Setting prohibited. Be sure value before using		Setting prohibited. Be sure to write any other value before using the PLL.					
			0	1	Sub clock x 2					
			1	0	Sub clock x 3					
	SPMC1. SPMC0:		1	1	Sub clock x 4					
bit2 bit1	multiplier setting bits (Two-system clock product only)		a single syster otes: Although the setting. Be sur oscillation ena clock control is These bits car update the bit system clock s [It is however	n clock produ initial value re to set the bi able bit (SPE) be updated of s either with selection bits possible to se	ct, the value of these bits has no effect on the op of these bits is $"00_B"$ , the PLL does not open ts to any value other than $"00_B"$ either before se N) to "1" or before setting the clock mode sele C:SCS1, SCS0) to $"01_B"$ . only when the sub PLL clock is stopped. Conse the sub PLL clock oscillation enable bit (SPEN in the system clock control register (SYCC:SC at these bits at the same time as setting SPEN to	peration. rate normally with this tting the sub PLL clock ction bits in the system quently, you should not l) set to "1" or with the S1, SCS0) set to "01 <sub>B</sub> ". "1".)				
bit0	SPRDY: Sub PLL clock oscillation stability bit (Two-system clock product only)	Ind · ' · ' · ' · ' · ' · ' · ' · '	dicates wheth When set to " PLL clock has When set to oscillation stal is bit is read- a single syster	er sub PLL cl '1", the SPRE s passed. "0", the SPR bilization wai only; any valu n clock produ	ock oscillation has become stable. DY bit indicates that the oscillation stabilizatio DY bit indicates that the clock controller is t state or that sub PLL clock oscillation has bee the attempted to be written is meaningless. ct, the value of the bit is meaningless.	n wait time for the sub in the sub PLL clock n stopped.				

#### Table 6.4-1 Functions of Bits in PLL Control Register (PLLC) (2 / 2)

# 6.5 Oscillation Stabilization Wait Time Setting Register (WATR)

This register is used to set the oscillation stabilization wait time.

#### ■ Configuration of Oscillation Stabilization Wait Time Setting Register (WATR)

Address <u>k</u>	oit7	bit6	bit5	bit4	bit3	bit2	<u>bit1 bit0</u> Initial value
0005н S	WT3	SWT2	SWT1	SWT0	MWT3	3 MWT2	MWT1 MWT0 11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W R/W
		MWT3	MWT2	MWT1	MWT0	Number of Cycles	Main Oscillation Clock FcH = 4 MHz
		1	1	1	1	2 <sup>14</sup> -2	(2 <sup>14</sup> -2)/Fсн About 4.10 ms
		1	1	1	0	2 <sup>13</sup> -2	(2 <sup>13</sup> -2)/Fсн About 2.05 ms
		1	1	0	1	2 <sup>12</sup> -2	(2 <sup>12</sup> -2)/Fсн About 1.02 ms
		1	1	0	0	2 <sup>11</sup> -2	(2 <sup>11</sup> -2)/Гсн 511.5 µs
		1	0	1	1	2 <sup>10</sup> -2	(2 <sup>10</sup> -2)/Fсн 255.5 μs
		1	0	1	0	2 <sup>9</sup> -2	(2 <sup>9</sup> -2)/Fсн 127.5 µs
	1	1	0	0	1	2 <sup>8</sup> -2	(2 <sup>8</sup> -2)/Fсн 63.5 µs
	1	1	0	0	0	2 <sup>7</sup> -2	(2 <sup>7</sup> -2)/Fсн 31.5 µs
	1	0	1	1	1	2 <sup>6</sup> -2	(2 <sup>6</sup> -2)/Fсн 15.5 µs
		0	1	1	0	2⁵-2	(2 <sup>5</sup> -2)/Fсн 7.5 µs
		0	1	0	1	2 <sup>4</sup> -2	(2 <sup>4</sup> -2)/Fсн 3.5 µs
		0	1	0	0	2 <sup>3</sup> -2	(2 <sup>3</sup> -2)/Fcн 1.5 µs
		0	0	1	1	2 <sup>2</sup> -2	(2 <sup>2</sup> -2)/EcH 0.5 US
		0	0	1	0	2 <sup>1</sup> -2	$(2^{1}-2)/F_{CH} = 0.0 \ \mu s$
		0	0	0	1	2 <sup>1</sup> -2	$(2^{1}-2)/F_{CH} = 0.0 \ \mu s$
		0	0	0	0	22 21_2	$(2^{1}-2)/F_{CH} = 0.0 \ \mu s$
		L	Ű	<u> </u>	Ŭ	2 -2	
	$ \longrightarrow $	SWT3	SWT2	SWT1	SWT0	Number of Cycles	Sub Oscillation Clock FcL = 32.768 kHz
		1	1	1	1	2 <sup>15</sup> -2	(2 <sup>15</sup> -2)/F <sub>CL</sub> About 1.00 s
		1	1	1	0	2 <sup>14</sup> -2	(2 <sup>14</sup> -2)/Fc∟ About 0.5 s
		1	1	0	1	2 <sup>13</sup> -2	(2 <sup>13</sup> -2)/Fc∟ About 0.25 s
		1	1	0	0	2 <sup>12</sup> -2	(2 <sup>12</sup> -2)/FcL About 0.125 s
		1	0	1	1	2 <sup>11</sup> -2	(2 <sup>11</sup> -2)/Fc∟ About 62.44 ms
		1	0	1	0	2 <sup>10</sup> -2	(2 <sup>10</sup> -2)/FcL About 31.19 ms
		1	0	0	1	2 <sup>9</sup> -2	(2 <sup>9</sup> -2)/FcL About 15.56 ms
		1	0	0	0	2 <sup>8</sup> -2	(2 <sup>8</sup> -2)/FcL About 7.75 ms
		0	1	1	1	2 <sup>7</sup> -2	(2 <sup>7</sup> -2)/F <sub>CL</sub> About 3.85 ms
		0	1	1	0	2 <sup>6</sup> -2	(2 <sup>6</sup> -2)/FcL About 1.89 ms
		0	1	0	1	2 <sup>5</sup> -2	(2⁵-2)/Fc∟ About 915.5 μs
		0	1	0	0	24-2	(2 <sup>4</sup> -2)/FcL About 427.2 μs
		0	0	1	1	2 <sup>3</sup> -2	(2 <sup>3</sup> -2)/Fc∟ About 183.1 μs
		0	0	1	0	2 <sup>2</sup> -2	(2 <sup>2</sup> -2)/FcL About 61.0 μs
		0	0	0	1	2 <sup>1</sup> -2	(2 <sup>1</sup> -2)/FcL 0.0 μs
		-					

Figure 6.5-1 Configuration of Oscillation Stabilization Wait Time Setting Register (WATR)

	Bit name	Function									
		Set the sub clock oscillation	stabilization v	wait time.							
		SWT3 SWT2 SWT1 SWT0	Number of Cycles	Sub clock F <sub>CL</sub>	= 32.768 kHz						
		1111 <sub>B</sub>	2 <sup>15</sup> -2	(2 <sup>15</sup> -2)/F <sub>CL</sub>	About 1.0 s						
		1110 <sub>B</sub>	2 <sup>14</sup> -2	$(2^{14}-2)/F_{CL}$	About 0.5 s						
		1101 <sub>B</sub>	2 <sup>13</sup> -2	(2 <sup>13</sup> -2)/F <sub>CL</sub>	About 0.25 s						
		1100 <sub>B</sub>	2 <sup>12</sup> -2	(2 <sup>12</sup> -2)/F <sub>CL</sub>	About 0.125 s						
		1011 <sub>B</sub>	2 <sup>11</sup> -2	(2 <sup>11</sup> -2)/F <sub>CL</sub>	About 62.44 ms						
		1010 <sub>B</sub>	2 <sup>10</sup> -2	(2 <sup>10</sup> -2)/F <sub>CL</sub>	About 31.19 ms						
		1001 <sub>B</sub>	2 <sup>9</sup> -2	(2 <sup>9</sup> -2)/F <sub>CL</sub>	About 15.56 ms						
		1000 <sub>B</sub>	2 <sup>8</sup> -2	(2 <sup>8</sup> -2)/F <sub>CL</sub>	About 7.75 ms						
	SWT3, SWT2,	0111 <sub>B</sub>	2 <sup>7</sup> -2	(2 <sup>7</sup> -2)/F <sub>CL</sub>	About 3.85 ms						
bit7 to	SWT1, SWT0: Sub clock oscillation	0110 <sub>B</sub>	2 <sup>6</sup> -2	(2 <sup>6</sup> -2)/F <sub>CL</sub>	About 1.89 ms						
bit4	stabilization wait time selection bits	0101 <sub>B</sub>	2 <sup>5</sup> -2	(2 <sup>5</sup> -2)/F <sub>CL</sub>	About 915.5 µs						
		0100 <sub>B</sub>	2 <sup>4</sup> -2	(2 <sup>4</sup> -2)/F <sub>CL</sub>	About 427.2 μs						
		0011 <sub>B</sub>	2 <sup>3</sup> -2	(2 <sup>3</sup> -2)/F <sub>CL</sub>	About 183.1 µs						
		0010 <sub>B</sub>	2 <sup>2</sup> -2	(2 <sup>2</sup> -2)/F <sub>CL</sub>	About 61.0 µs						
		0001 <sub>B</sub>	2 <sup>1</sup> -2	(2 <sup>1</sup> -2)/F <sub>CL</sub>	0.0 µs						
		0000 <sub>B</sub>	2 <sup>1</sup> -2	(2 <sup>1</sup> -2)/F <sub>CL</sub>	0.0 µs						
		On single system clock product Number of cycles in the above t above table for a maximum value Note: Do not update these b update them either wi register (SYCC:SRD) also update them whill system clock control r clock mode.	t, the value of th table is for a min ue. its during sub cl th the sub clock Y) set to "1" or i e the sub clock i register (SYCC:	ese bits is meaningless imum value. Add 1/F <sub>C</sub> lock oscillation stabiliz oscillation stability bi n sub clock mode or si s stopped with the sub SUBS) set to "1" in ma	3. <sub>2L</sub> to the number of cy zation wait time. You t in the system clock ub PLL clock mode. <sup>2</sup> clock oscillation stop ain clock mode or ma	ycle in the should control You can bit in the ain PLL					

#### Table 6.5-1 Functions of Bits in Oscillation Stabilization Wait Time Setting Register (WATR) (1 / 2)
Bit name		Function							
		Set the main clock oscillation stabilization wait time.							
		MWT3 MWT2 MWT1 MWT0	Number of Cycles	Main clock F <sub>CH</sub> = 4 MHz					
		1111 <sub>B</sub>	2 <sup>14</sup> -2	$(2^{14}-2)/F_{CH}$	About 4.10 ms				
		1110 <sub>B</sub>	2 <sup>13</sup> -2	$(2^{13}-2)/F_{CH}$	About 2.05 ms				
		1101 <sub>B</sub>	2 <sup>12</sup> -2	$(2^{12}-2)/F_{CH}$	About 1.02 ms				
		1100 <sub>B</sub>	2 <sup>11</sup> -2	$(2^{11}-2)/F_{CH}$	511.5 μs				
		1011 <sub>B</sub>	2 <sup>10</sup> -2	$(2^{10}-2)/F_{CH}$	255.5 μs				
		1010 <sub>B</sub>	2 <sup>9</sup> -2	(2 <sup>9</sup> -2)/F <sub>CH</sub>	127.5 μs				
		1001 <sub>B</sub>	2 <sup>8</sup> -2	$(2^{8}-2)/F_{CH}$	63.5 μs				
bit3 MWT3, MW	Γ2, Γ0:	1000 <sub>B</sub>	2 <sup>7</sup> -2	$(2^{7}-2)/F_{CH}$	31.5 µs				
to Main clock os	scillation	0111 <sub>B</sub>	2 <sup>6</sup> -2	$(2^{6}-2)/F_{CH}$	15.5 μs				
selection bits		0110 <sub>B</sub>	2 <sup>5</sup> -2	$(2^{5}-2)/F_{CH}$	7.5 μs				
		0101 <sub>B</sub>	2 <sup>4</sup> -2	$(2^{4}-2)/F_{CH}$	3.5 µs				
		0100 <sub>B</sub>	2 <sup>3</sup> -2	$(2^{3}-2)/F_{CH}$	1.5 µs				
		0011 <sub>B</sub>	2 <sup>2</sup> -2	$(2^2-2)/F_{CH}$	0.5 µs				
		0010 <sub>B</sub>	2 <sup>1</sup> -2	$(2^{1}-2)/F_{CH}$	0.0 µs				
		0001 <sub>B</sub>	2 <sup>1</sup> -2	$(2^{1}-2)/F_{CH}$	0.0 µs				
		0000 <sub>B</sub>	2 <sup>1</sup> -2	$(2^{1}-2)/F_{CH}$	0.0 µs				

### Table 6.5-1 Functions of Bits in Oscillation Stabilization Wait Time Setting Register (WATR) (2 / 2)

# 6.6 Standby Control Register (STBC)

The standby control register (STBC) is used to control transition from the RUN state to sleep mode, stop mode, timebase timer mode, or watch mode, set the pin state in stop mode, timebase timer mode, and watch mode, and to control the generation of software resets.

### Standby Control Register (STBC)

Address	s biť	7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	
0008 <sub>H</sub>	S	TP	SLP	SPL	SRS	T TMD	-	-	-	0000000B	
	R	),W	R0,W	R/W	R0,W	/ RQ,W	R0/WX	R0/WX	R0/WX		
		[	1								
		TMD					Watch b	it			
			R	ead				Write	9		
		0	Alway "0".	s reads			Has no e	ffect on t	he operati	on.	
						Main c	ock mode	Э.	Subclo	ck mode	
		1		-		Main PLL	. clock mo	ode	Sub PLL	clock mode	
		-				Causes t	ransition	to	Causes t	ransition to	
						timebase	timer mo	de	watcl	n mode	
			1			0					
	$ \rightarrow $	SRST		Da		Software reset bit					
			Read			VVIIte					
		1	Always reads "0".			Cana	Constrates a 2 machine cleak reset signal				
		I		- Generates a 3 machine clock reset signal							
	>	SPL	Pin state setting bit								
		0	Holds external pins in their immediately preceding state in stop mode, timebase timer mode, or watch mode								
		1	Places external pins in a high impedance state in stop mode, timebase timer mode, or watch mode.								
	I										
						S	leep bit	ep bit			
	$\rightarrow$	SLP		Re	ad				Write		
		0	Alv	vays rea	ads "0".		F	Has no effect on the operation			
		1			-		C	auses tra	ansition to	sleep mode	
						S	stop bit				
	-			Re	ad				Write		
		0	Alv	vays rea	ads "0".		F	las no el	fect on the	e operation	
		1			-		C	auses tr	ansition to	stop mode	
R0,W R/W R0/WX -	: Write : Reada : Undef : Unuse : Initial	only (Wr able/writa fined bit ed value	itable, "0" able (Rea (Read val	is read) d value is ue is "0", v	the same writing ha	e as write va as no effect o	lue) on operation	)			

Figure 6.6-1 Standby Control Register (STBC)

	Bit Name	Function
bit7	STP: Stop bit	<ul> <li>Sets transition to stop mode.</li> <li>When set to "0": the bit is meaningless.</li> <li>When set to "1": the bit causes transition to stop mode.</li> <li>When read, the bit always returns "0".</li> <li>Note: An attempt to write "1" to this bit is ignored if an interrupt request has been issued. For details, see "6.8.1 Notes on Using Standby Mode".</li> </ul>
bit6	SLP: Sleep bit	<ul> <li>Sets transition to sleep mode.</li> <li>When set to "0": the bit is meaningless.</li> <li>When set to "1": the bit causes transition to sleep mode.</li> <li>When read, the bit always returns "0".</li> <li>Note: An attempt to write "1" to this bit is ignored if an interrupt request has been issued. For details, see "6.8.1 Notes on Using Standby Mode".</li> </ul>
bit5	SPL: Pin state setting bit	<ul> <li>Sets the states of external pins in stop mode, timebase timer mode, and watch mode.</li> <li>When set to "0": the bit holds the states (levels) of external pins in stop mode, timebase timer mode, and watch mode.</li> <li>When set to "1": the bit places external pins in a high impedance state in stop mode, timebase timer mode, and watch mode. (Those pins are pulled up for which pull-up resistor connection has been selected in the pull-up setting register.)</li> </ul>
bit4	SRST: Software reset bit	Sets a software reset. When set to "0": the bit is meaningless. When set to "1": the bit generates a 3 machine clock reset signal. When read, the bit always returns "0".
bit3	TMD: Watch bit	<ul> <li>On two-system clock product, this bit sets transition to timebase timer mode or watch mode.</li> <li>On single system clock product, the bit sets transition to timebase timer mode.</li> <li>Writing "1" to the bit in main clock mode or main PLL clock mode causes transition to timebase timer mode.</li> <li>Writing "1" to the bit in sub clock mode or sub PLL clock mode causes transition to watch mode.</li> <li>Writing "0" to the bit is meaningless.</li> <li>When read, the bit always returns "0".</li> <li>Note: An attempt to write "1" to this bit is ignored if an interrupt request has been issued. For details, see "6.8.1 Notes on Using Standby Mode".</li> </ul>
bit2 to bit0	Unused bits	When read, these bits always return "0". These are unused bits. The bits are read-only; any value attempted to be written is meaningless.

Table 6.6-1 Functions of Bits in Standby Control Register (STBC)

Notes:

- Set the standby mode after making sure that the transition to clock mode has been completed by comparing the values of the clock mode monitor bits (SYCC:SCM1,SCM0) and clock mode setting bits (SYCC:SCS1,SCS0) in the system clock control register.
- If you write "1" simultaneously to two or more of the stop bit (STP), sleep bit (SLP), software reset bit (SRST), and watch bit (TMD), priority is given to them in the following order:
  - (1) Software reset bit (SRST)
  - (2) Stop bit (STP)
  - (3) Watch bit (TMD)
  - (4) Sleep bit (SLP)

When released from the standby mode, the device returns to the normal operating status.

### 6.7 Clock Modes

The clock modes available are: main clock mode, sub clock mode, main PLL clock mode, and sub PLL clock mode. Mode switching takes place according to the settings in the system clock control register (SYCC).

Sub clock mode and sub PLL clock mode are not supported by single system clock product.

### Operations in Main Clock Mode

Main clock mode uses the main clock as the machine clock for the CPU and peripheral resources.

The timebase timer operates with the main clock.

The watch prescaler and watch counter operate with the sub clock (on two-system clock product).

If you set standby mode during operation in main clock mode, the device can enter sleep mode, stop mode, or timebase timer mode.

After a reset, main clock mode is always set regardless of the clock mode used before the reset.

### Operations in Sub Clock Mode (on Two-system Clock Product)

Sub clock mode uses the sub clock as the machine clock for the CPU and peripheral resources with main clock oscillation stopped. In this mode, the timebase timer remains stopped as it requires the main clock for operation.

If you set standby mode during operation in sub clock mode, the device can enter sleep mode, stop mode, or watch mode.

### Operations in Main PLL Clock Mode

Main PLL clock mode uses the main PLL clock as the machine clock for the CPU and peripheral resources. The timebase timer and watchdog timer operate with the main clock.

The watch prescaler and watch counter operate with the sub clock (on two-system clock product).

If you set standby mode during operation in main PLL clock mode, the device can enter sleep mode, stop mode, or timebase timer mode.

### Operations in Sub PLL Clock Mode (on Two-system Clock Product)

Sub PLL clock mode uses the sub PLL clock as the machine clock for the CPU and peripheral resources with main clock oscillation stopped. In this mode, the timebase timer remains stopped as it requires the main clock for operation. The watch prescaler and watch counter operate with the sub clock.

If you set standby mode during operation in sub PLL clock mode, the device can enter sleep mode, stop mode, or watch mode.

### ■ Clock Mode State Transition Diagram

The clock modes available are: main clock mode, main PLL clock mode, sub clock mode, and sub PLL clock mode. The device can switch between these modes according to the settings in the system clock control register (SYCC).



Figure 6.7-1 Clock Mode State Transition Diagram (Two-system Clock Product)



Figure 6.7-2 Clock Mode State Transition Diagram (Single System Clock Product)

	Current State	Next State	Description
<1>	Reset state	Main clock	After a reset, the device waits for the main clock oscillation stabilization wait time to elapse and enters main clock mode. If the reset is a watchdog reset, software reset, or external reset caused in main clock mode or main PLL clock mode, however, the device does not wait for
(1)			the main clock oscillation stabilization wait time to elapse. The device enters sub clock mode when the system clock selection bits in the system clock control register (SYCC: SCS1, SCS0) are set to " $00_B$ ".
(2)		Sub clock	Note, however, that the device waits for the sub clock oscillation stabilization wait time to elapse before entering sub clock mode either if the sub clock has been stopped according to the setting of the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS) in main clock mode or if the sub clock oscillation stabilization wait time has not passed immediately after the power is turned on.
(3)	Main clock	Sub PLL clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to $"01_B"$ , the device enters sub PLL clock mode after waiting for the sub PLL clock oscillation stabilization wait time. Note, however, that the device does not wait for the sub PLL clock oscillation stabilization wait time to elapse if the sub PLL clock has been oscillating according to the setting of the sub PLL clock oscillation enable bit in the PLL control register (PLLC: SPEN) in main clock mode. Note also that the device waits for the sub clock oscillation stabilization wait time to elapse before entering sub PLL clock mode
(4)			either if the sub clock has been stopped according to the setting of the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS) in main clock mode or if the sub clock oscillation stabilization wait time has not passed immediately after the power is turned on. When the device waits for the sub clock oscillation stabilization wait time or sub PLL clock oscillation stabilization wait time, it waits for whichever is longer to elapse.
(5)		Main PLL clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to "11", the device enters main PLL clock mode after waiting for the main PLL clock oscillation stabilization wait time. Note, however, that the device does not wait for the main
(6)			PLL clock oscillation stabilization wait time to elapse if the main PLL clock has been oscillating according to the setting of the main PLL clock oscillation enable bit in the PLL control register (PLLC: MPEN).

Table 6.7-1 Clock Mode State Transition Table (1 / 2)

Table 6.7-1	Clock Mode	State	Transition	Table	(2 / 2)
-------------	------------	-------	------------	-------	---------

	Current State	Next State	Description
(7)		Main clock	The device enters main clock mode when the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $10_B$ ".
(8)			The device enters sub clock mode when the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $00_B$ ".
(9)		Sub clock	Note, however, that the device waits for the sub clock oscillation stabilization wait time to elapse before entering sub clock mode either if the sub clock has been stopped according to the setting of the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS) in main PLL clock mode or if the sub clock oscillation stabilization wait time has not passed immediately after the power is turned on.
(10)	Main PLL clock		When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $01_B$ ", the device enters sub PLL clock mode after waiting for the sub PLL clock oscillation stabilization wait time. Note, however, that the device does not wait for the sub PLL clock oscillation stabilization wait time to elapse if the sub PLL clock has been oscillating according to the setting of the sub PLL clock oscillation enable bit in the PLL control register (PLLC: SPEN) in main PLL clock mode.
(11)		Sub PLL clock	Note also that the device waits for the sub clock oscillation stabilization wait time to elapse before entering sub PLL clock mode either if the sub clock has been stopped according to the setting of the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS) in main PLL clock mode or if the sub clock oscillation stabilization wait time has not passed immediately after the power is turned on. When the device waits for the sub clock oscillation stabilization wait time or sub PLL clock oscillation stabilization wait time, it waits for whichever is longer to elapse.
(12)		Main clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $10_B$ ", the device enters main clock mode after waiting for the main clock oscillation stabilization wait time.
(13)		Cych DI L alock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $01_B$ ", the device enters sub PLL clock mode after waiting for the sub PLL clock oscillation stabilization wait time. Note, however, that the device does not wait for the sub
(14)	Sub clock	Sub PLL clock	PLL clock oscillation stabilization wait time to elapse if the sub PLL clock has been oscillating according to the setting of the sub PLL clock oscillation enable bit in the PLL control register (PLLC: SPEN) in sub clock mode.
(15)		Main PLL clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $11_B$ ", the device enters main PLL clock mode after waiting for the main PLL clock oscillation stabilization wait time or main clock oscillation stabilization wait time to elapse, whichever is longer.
(16)		Sub clock	The device enters sub clock mode when the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $00_B$ ".
(17)	Sub PLL clock	Main PLL clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $11_B$ ", the device enters main PLL clock mode after waiting for the main PLL clock oscillation stabilization wait time or main clock oscillation stabilization wait time to elapse, whichever is longer.
(18)		Main clock	When the system clock selection bits in the system clock control register (SYCC: SCS1, 0) are set to " $10_B$ ", the device enters main clock mode after waiting for the main clock oscillation stabilization wait time.

# 6.8 Operations in Low-power Consumption Modes (Standby Modes)

# The standby modes available are: sleep mode, stop mode, timebase timer mode, and watch mode.

### Overview of Transitions to and from Standby Mode

The standby modes available are: sleep mode, stop mode, timebase timer mode, and watch mode. The device enters standby mode according to the settings in the standby control register (STBC).

The device is released from standby mode in response to an interrupt or reset. Before transition to normal operation, the device waits for the oscillation stabilization wait time to elapse as required.

When released from standby mode by a reset, the device returns to main clock mode. When released from standby mode by an interrupt, the device enters the clock mode in which the device was before entering the standby mode.

### Pin States in Standby Mode

The pin state setting bit (STBC:SPL) of the standby control register can be used to set the I/O port/ peripheral resource pins in the stop mode, timebase timer mode, or watch mode to hold their immediately preceding state or to be placed in a high impedance state.

See "APPENDIX D Pin Status of MB95130/M series" for the states of all pins in standby modes.

### 6.8.1 Notes on Using Standby Mode

Even if the standby control register (STBC) sets standby mode, transition to the standby mode does not take place when an interrupt request has been issued from a peripheral resource. When the device returns from standby mode to the normal operating state in response to an interrupt, the operation that follows varies depending on whether the interrupt request is accepted or not.

### Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction.

The device requires four machine clock cycles before entering standby mode after it is set in the standby control register. During that period, the CPU executes the program. To avoid program execution during this transition to standby mode, enter at least three NOP instructions.

The device operates normally if you place instructions other than NOP instructions. In that case, however, note that the device may execute the instructions to be executed after being released from standby mode before entering the standby mode and that the device may enter the standby mode during instruction execution, which is resumed after the device is released from the standby mode (increasing the number of instruction execution cycles).

### Check That Clock-mode Transition has been Completed before Setting Standby Mode.

Before setting standby mode, make sure that clock-mode transition has been completed by comparing the values of the clock mode monitor bit (SYCC: SCM1, 0) and clock mode setting bit (SYCC: SCS1, 0) in the system clock control register.

### An Interrupt Request may Suppress Transition to Standby Mode.

If an attempt is made to set a standby mode while an interrupt request with an interrupt level higher than " $11_B$ " has been issued, the device ignores the attempt to write to the standby control register and continues instruction execution without entering the standby mode. The device does not enter the standby mode even after having serviced the interrupt.

This behavior is the same as when interrupts are disabled by the interrupt enable flag (CCR:I) and interrupt level bits in the condition code register (CCR:IL 1,0) of the CPU.

### Standby Mode is Also Canceled when the CPU Rejects Interrupts.

When an interrupt request with an interrupt level higher than " $11_B$ " is issued in standby mode, the device is released from the standby mode regardless of the settings of the interrupt enable flag (CCR: I) and interrupt level bits (CCR:IL1,0) of the condition code register of the CPU.

After being released from standby mode, the device services the interrupt when the CPU's condition code register has been set to accept interrupts. If the register has been set to reject interrupts, the device resumes processing from the instruction that follows the last instruction executed before entering the standby mode.

### ■ Standby Mode State Transition Diagram

Figure 6.8-1 and Figure 6.8-2 are standby mode state transition diagrams.



### Figure 6.8-1 Standby Mode State Transition Diagram (Two-system Clock Product)



Figure 6.8-2 Standby Mode State Transition Diagram (Single System Clock Product)

	State Transition	Description
<1>		After a reset, the device enters main clock mode. If the reset is a power-on reset, the device always waits for the main clock oscillation stabilization wait time to elapse. When the clock mode before the reset is sub clock mode or sub PLL clock mode, the device waits
<2>	Normal operation from reset state	for the main clock oscillation stabilization wait time to elapse. The device waits for it as well when the standby mode is stop mode. When the clock mode before the reset is main clock mode or main PLL clock mode and the standby mode is other than stop mode, the device does not wait for the main clock oscillation stabilization wait time to elapse even after entering a reset state in response to a watchdog reset, software reset, or external reset.
(1)	Sleep mode	The device enters sleep mode when "1" is written to the sleep bit in the standby control register (STBC: SLP).
(2)		The device returns to the RUN state in response to an interrupt from a peripheral resource.
(3)		The device enters stop mode when "1" is written to the stop bit in the standby control register (STBC: STP).
(4)	Stop mode	In response to an external interrupt, the device returns to the RUN state after waiting for the oscillation stabilization wait time required for each clock mode. When the device waits for a PLL oscillation stabilization wait time, it waits for the relevant oscillation stabilization wait time or PLL oscillation stabilization wait time to elapse, whichever is longer.
(5)		The device enters timebase timer mode when "1" is written to the watch bit in the standby control register (STBC: TMD) in main clock mode or main PLL clock mode.
(6)	Timebase timer mode	The device returns to the RUN state in response to a timebase timer interrupt, watch prescaler/ watch counter interrupt, or external interrupt. When the clock mode is main PLL clock mode, the device waits for the main PLL clock oscillation stabilization wait time to elapse. If the main PLL oscillation enable bit in the PLL control register
(7)		(PLLC: MPEN) contains "1", however, the device does not wait for that time to elapse even when the clock mode is main PLL clock mode.
(8)		The device enters watch mode when "1" is written to the watch bit in the standby control register (STBC: TMD) in sub clock mode or sub PLL clock mode.
(9)	Watch mode	The device returns to the normal operating state in response to a watch prescaler/watch counter interrupt or external interrupt. When the clock mode is sub PLL clock mode, the device waits for the sub PLL clock oscillation
(10)		(PLLC: SPEN) contains "1", however, the device does not wait for that time to elapse even when the clock mode is sub PLL clock mode.

 Table 6.8-1
 State Transition Diagram (Transitions to and from Standby Modes)

## 6.8.2 Sleep Mode

### Sleep mode stops the operations of the CPU and watchdog timer.

### ■ Operations in Sleep Mode

Sleep mode stops the operating clock for the CPU and watchdog timer. In this mode, the CPU stops while retaining the contents of registers and RAM that exist immediately before the transition to sleep mode, but the peripheral resources except the watchdog timer continue operating.

### • Transition to sleep mode

Writing "1" to the sleep bit in the standby control register (STBC:SLP) causes the device to enter sleep mode.

### • Cancellation of sleep mode

A reset or an interrupt from a peripheral resource releases the device from sleep mode.

### 6.8.3 Stop Mode

### Stop mode stops the main clock.

### Operations in Stop Mode

Stop mode stops the main clock. In this mode, the device stops all the functions except external interrupt and low-voltage detection reset while retaining the contents of registers and RAM that exist immediately before the transition to stop mode.

In main clock mode or main PLL clock mode, however, you can start or stop sub clock oscillation by setting the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS). When the sub clock is oscillating, the watch prescaler and watch counter operate.

#### Transition to stop mode

Writing "1" to the stop bit in the standby control register (STBC:STP) causes the device to enter stop mode. At this time, the states of external pins are retained when the pin state setting bit in the standby control register (STBC:SPL) is "0", and the states of external pins become high impedance when that bit is "1" (those pins are pulled up for which pull-up resistor connection has been selected in the pull-up setting register).

In main clock mode or main PLL clock mode, a timebase timer interrupt request may be generated while the device is waiting for main clock oscillation to stabilize after being released from stop mode by an interrupt. If the interrupt interval time of the timebase timer is shorter than the main clock oscillation stabilization wait time, you should disable interrupt requests output from the timebase timer before entering stop mode, thereby preventing unexpected interrupts from occurring.

You should also disable interrupt requests output from the watch prescaler before entering stop mode in sub clock mode or sub PLL clock mode.

#### Cancellation of stop mode

The device is released from stop mode in response to a reset or an external interrupt.

In main clock mode or main PLL clock mode, you can start or stop sub clock oscillation by setting the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS). When the sub clock is oscillating, you can also release the device from stop mode using an interrupt by the watch prescaler or watch counter.

Note:

When stop mode is canceled via an interrupt, peripheral resources placed into stop mode during an action resume that action. Therefore, the initial interval time of the interval timer and other similar settings are rendered indeterminate. After recovery from stop mode, initialize each peripheral resource as necessary.

## 6.8.4 Timebase Timer Mode

# Timebase timer mode allows only the main clock oscillation, sub clock oscillation, timebase timer, and watch prescaler to work. The operating clock for the CPU and peripheral resources is stopped in this mode.

### Operations in Timebase Timer Mode

In timebase timer mode, main clock supply is stopped except for the timebase timer. The device stops all the functions except timebase timer, external interrupt and low-voltage detection reset while retaining the contents of registers and RAM that exist immediately before the transition to timebase timer mode.

You can however start or stop sub clock oscillation by setting the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS). When the sub clock is oscillating, the watch prescaler and watch counter operate.

### Transition to timebase timer mode

Writing "1" to the watch bit in the standby control register (STBC:TMD) causes the device to enter timebase timer mode if the system clock monitor bits in the system clock control register (SYCC: SCM1, SCM0) are " $10_B$ " or " $11_B$ ".

The device can enter timebase timer mode only when the clock mode is main clock mode or main PLL clock mode.

Upon transition to timebase timer mode, the states of external pins are retained when the pin state setting bit in the standby control register (STBC:SPL) is "0", and the states of external pins become high impedance when that bit is "1" (those pins are pulled up for which pull-up resistor connection has been selected in the pull-up setting register).

### Cancellation of timebase timer mode

The device is released from timebase timer mode in response to a reset, timebase timer interrupt, or external interrupt.

You can start or stop sub clock oscillation by setting the sub clock oscillation stop bit in the system clock control register (SYCC: SUBS). When the sub clock is oscillating, you can also release the device from timebase timer mode using an interrupt by the watch prescaler or watch counter.

Note:

When timebase timer mode is canceled via an interrupt, peripheral resources placed into timebase timer mode during an action resume that action. Therefore, the initial interval time of the interval timer and other similar settings are rendered indeterminate. After recovery from timebase timer mode, initialize each peripheral resource as necessary.

### 6.8.5 Watch Mode

# Watch mode allows only the sub clock and watch prescaler to work. The operating clock for the CPU and peripheral resources is stopped in this mode.

### Operations in Watch Mode

In watch mode, the operating clock for the CPU and peripheral resources is stopped. The device stops all the functions except the watch prescaler, watch counter, external interrupt, and low-voltage detection reset while retaining the contents of registers and RAM that exist immediately before the transition to watch mode.

### Transition to watch mode

Writing "1" to the watch bit in the standby control register (STBC:TMD) causes the device to enter watch mode if the system clock monitor bits in the system clock control register (SYCC: SCM1, SCM0) are " $00_B$ " or " $01_B$ ".

The device can enter watch mode only when the clock mode is sub clock mode or sub PLL clock mode. Upon transition to watch mode, the states of external pins are retained when the pin state setting bit in the standby control register (STBC:SPL) is "0", and the states of external pins become high impedance when that bit is "1" (those pins are pulled up for which pull-up resistor connection has been selected in the pull-up setting register).

### Cancellation of watch mode

The device is released from watch mode in response to a reset, watch interrupt, or external interrupt.

Note:

When watch mode is canceled via an interrupt, peripheral resources placed into watch mode during an action resume that action. Therefore, the initial interval time of the interval timer and other similar settings are rendered indeterminate. After recovery from watch mode, initialize each peripheral resource as necessary.

# 6.9 Clock Oscillator Circuits

The clock oscillator circuit generates an internal clock with an oscillator connected to or a clock signal input to the clock oscillation pin.

### Clock Oscillator Circuit

• Using crystal and ceramic oscillators

Connect crystal and ceramic oscillators as shown in Figure 6.9-1.



### Figure 6.9-1 Sample Connections of Crystal and Ceramic Oscillators

• Using external clock

As shown in Figure 6.9-2, connect the external clock to the X0 pin while leaving the X1 pin open. To supply the sub clock from an external source, connect the external clock to the X0A pin while leaving the X1A pin open.



### Figure 6.9-2 Sample Connections of External Clocks

Note:

If you use only the main clock without using sub clock oscillation on a two-system clock product and it enters sub clock mode for some reason, there is no solution to recovering its operation as there is no clock supply available. If you use the main clock alone, therefore, be sure to select a single system clock product.

## 6.10 Overview of Prescaler

# The prescaler generates the count clock source for various peripheral resources from the machine clock (MCLK) and the count clock output from the time-base timer.

### Prescaler

The prescaler generates the count clock source for various peripheral resources from the machine clock (MCLK) that drives the CPU and the count clock  $(2^7/F_{CH} \text{ or } 2^8/F_{CH})$  output from of the time-base timer. The count clock source is a clock frequency-divided by the prescaler or a buffered clock, used by the peripheral resources listed below.

Note that the prescaler has no control register and operates continuously driven by the machine clock (MCLK) and the count clock  $(2^7/F_{CH} \text{ or } 2^8/F_{CH})$  of the timebase timer.

- 8/16-bit compound timer 0
- 8/16-bit PPG timer 0, 1
- 16-bit PPG timer 0
- UART/SIO baud rate generator 0
- 8/10-bit A/D converter

#### 6.11 **Configuration of Prescaler**

### Figure 6.11-1 is a block diagram of the prescaler.

### Prescaler Block Diagram



Figure 6.11-1 Prescaler Block Diagram

• 5-bit counter

The machine clock (MCLK) is counted by a 5-bit counter and the count value is output to the output control circuit.

• Output control circuit

Based on the 5-bit counter value, this circuit supplies clocks generated by frequency-dividing the machine clock (MCLK) by 2, 4, 8, 16, or 32 to individual peripheral resources. The circuit also buffers the clock from the timebase timer  $(2^7/F_{CH} \text{ and } 2^8/F_{CH})$  and supplies it to the peripheral resources.

### Input Clock

The prescaler uses the machine clock or the clock output from the timebase timer as the input clock.

### Output Clock

The prescaler supplies clocks to the 8/10-bit compound timer, 8/16-bit PPG timer, 16-bit PPG timer, UART/SIO dedicated baud rate generator, and 8/10-bit A/D converter.

# 6.12 Operating Explanation of Prescaler

### The prescaler generates count clock sources to individual peripheral resources.

### Operations of Prescaler

The prescaler generates count clock sources from the frequency-divided version of the machine clock (MCLK) and buffered signals from the timebase timer  $(2^7/F_{CH}, 2^8/F_{CH})$  and supplies them to individual peripheral resources. The prescaler remains operating as long as the machine clock and timebase timer clocks are supplied.

Table 6.12-1 lists the count clock sources generated by the prescaler.

Count Clock Source Cycle	Cycle (F <sub>CH</sub> =10MHz, MCLK=10MHz)		Cycle (F <sub>CF</sub> MCLK=	<sub>l</sub> =16MHz, 16MHz)	Cycle (F <sub>CH</sub> =16.25MHz, MCLK=16.25MHz)		
2/MCLK	MCLK/2	(5MHz)	MCLK/2	(8MHz)	MCLK/2	(8.125MHz)	
4/MCLK	MCLK/4	(2.5MHz)	MCLK/4	(4MHz)	MCLK/4	(4.0625MHz)	
8/MCLK	MCLK/8	(1.25MHz)	MCLK/8	(2MHz)	MCLK/8	(2.0313MHz)	
16/MCLK	MCLK/16	(0.625MHz)	MCLK/16	(1MHz)	MCLK/16	(1.0156MHz)	
32/MCLK	MCLK/32	(0.3125MHz)	MCLK/32	(0.5MHz)	MCLK/32	(0.5078MHz)	
2 <sup>7</sup> / F <sub>CH</sub>	$F_{CH}/2^7$	(78kHz)	$F_{CH}/2^7$	(125kHz)	$F_{CH}/2^7$	(127kHz)	
2 <sup>8</sup> / F <sub>CH</sub>	$F_{CH}/2^8$	(39kHz)	$F_{CH}/2^8$	(62.5kHz)	$F_{CH}/2^8$	(63.5kHz)	

Table 6.12-1 Count Clock Sources Generated by Prescaler

# 6.13 Notes on Use of Prescaler

### This section gives notes on using the prescaler.

The prescaler uses the machine clock and timebase timer clock and operates continuously while these clocks are running. Accordingly, the operations of individual peripheral resources immediately after they are activated may involve an error of up to one cycle of the clock source captured by the resource, depending on the prescaler output value.

Figure 6.13-1 Clock Capturing Error Immediately after Activation of Peripheral Resources



The prescaler count value affects the following resources:

- UART/SIO
- 8/16-bit compound timer
- 8/16-bit PPG
- 16-bit PPG
- 8/10-bit A/D converter

# CHAPTER 7 RESET

This section describes the reset operation.

- 7.1 Reset Operation
- 7.2 Reset Source Register (RSRR)

# 7.1 Reset Operation

When a reset factor occurs, the CPU stops the current execution immediately and enters the reset release wait state. When the device is released from the reset, the CPU reads mode data and the reset vector from internal ROM (mode fetch). When the power is turned on or when the device is released from a reset in sub clock mode, sub-PLL clock mode, or stop mode, the CPU performs mode fetch after the oscillation stabilization wait time has passed.

### Reset Factors

Resets are classified into four reset factors.

Reset Factor	Reset Condition
External reset	"L" level input to the external reset pin
Software reset	"1" is written to the software reset bit (STBC: SRST) in the standby control register.
Watchdog reset	The watchdog timer causes an overflow.
Power-on reset/ low-voltage detection reset	The power is turned on or the supply voltage falls below the detected voltage. (Option)

#### Table 7.1-1 Reset Factors

### External reset

An external reset is generated upon "L" level input to the external reset pin ( $\overline{RST}$ ).

An externally input reset signal is accepted asynchronously via the internal noise filter and generates an internal reset signal in synchronization with the machine clock to initialize the internal circuit. Consequently, a clock is necessary for internal circuit initialization. Clock input is therefore necessary for operation with an external clock. Note, however, that external pins (including I/O ports and peripheral resources) are reset asynchronously. Additionally, there are standard pulse-width values for external reset input. If the value is below the standard, the reset may not be accepted.

The standard value is listed on the data sheet. Please design your external reset circuit so that this standard is met.

### Software reset

Writing "1" to the software reset bit of the standby control register (STBC:SRST) generates a software reset.

### Watchdog reset

After the watchdog timer starts, a watchdog reset is generated if the watchdog timer is not cleared within a preset amount of time.

#### Power-on reset/low-voltage detection reset (Option)

A power-on reset is generated when the power is turned on.

Some 5V products have a low-voltage detection reset circuit (option) integrated.

The low-voltage detection reset circuit generates a reset if the power supply voltage falls below a predetermined level.

The logical function of the low-voltage detection reset is completely equivalent to the power-on reset. All the text in this manual concerning power-on resets applies to low-voltage detection resets as well.

For details about low-voltage detection resets, see "CHAPTER 24 LOW-VOLTAGE DETECTION RESET CIRCUIT".

### Reset Time

In the case of a software reset or watchdog reset, the reset time consists of a total of three machine clock cycles: one machine clock cycle at the machine clock frequency selected before the reset, and two machine clock cycles at the machine clock frequency initially set after the reset (1/32 of the main clock frequency). However, the reset time may be extended in machine clock cycles of the frequency selected before the reset, via the RAM access protection function which suppresses resets during RAM access. In addition, when in main clock oscillation stabilization standby mode, the reset time is further extended for the oscillation stabilization wait time.

External resets and resets are also affected by the RAM access protection function and main clock oscillation stabilization wait time.

In the case of a power-on reset or low-voltage detection reset, the reset continues during the oscillation stabilization wait time.

### Reset Output

The reset pin of 5V products with the reset (For details, see Table 1.2-1.) outputs "L" level during reset time. However, a reset pin does not output "L" level in the case of an external reset.

The reset pin of 3V products and 5V products without the reset outputs do not have an output function.

### Overview of Reset Operation



Figure 7.1-1 Reset Operation Flow

In the case of a power-on reset/low-voltage detection reset, and a reset when in sub clock mode, sub-PLL clock mode, or stop mode, the CPU performs mode fetch after the main clock oscillation stabilization wait time has elapsed. If the external reset input is not cleared after the oscillation stabilization wait time has elapsed, the CPU performs mode fetch after the external reset input is cleared.

### Effect of Reset on RAM Contents

When a reset occurs, the CPU halts the operation of the command currently being executed, and enters the reset status. During RAM access execution, however, RAM access protection causes an internal reset signal to be generated in synchronization with the machine clock, after RAM access has ended. This function prevents a word-data write operation from being cut off by a reset after one byte.

### Pin State During a Reset

When a reset occurs, all of the I/O ports and peripheral resource pins remain in a high impedance state until setup is performed by software after the reset is released.

### Note:

Connect a pull-up resistor to those pins which remain at high impedance during a reset to prevent the devices the pins from malfunctioning.

See "APPENDIX D Pin Status of MB95130/M series" for details about the states of all pins during a reset.

# 7.2 Reset Source Register (RSRR)

# The reset source register indicates the source or factor causing a reset that has been generated.

### ■ Configuration of Reset Source Register (RSRR)



Figure 7.2-1 Reset Source Register (RSRR)

	Bit Name	Function
bit7 bit6 bit5	Unused bits	The value read is always 0. These bits are read-only. Any value written is meaningless.
bit4	EXTS: External reset flag bit	<ul> <li>This bit is set to "1" to indicate that an external reset has occurred.</li> <li>Otherwise, the bit retains the value existing before the reset occurred.</li> <li>Read access to this bit sets it to "0".</li> <li>The bit is read-only. Any value written is meaningless.</li> </ul>
bit3	WDTR: Watchdog reset flag bit	<ul> <li>This bit is set to "1" to indicate that a watchdog reset has occurred.</li> <li>Otherwise, the bit retains the value existing before the reset occurred.</li> <li>Read access to this bit sets it to "0".</li> <li>The bit is read-only. Any value written is meaningless.</li> </ul>
bit2	PONR: Power-on reset flag bit	<ul> <li>This bit is set to "1" to indicate that a power-on reset or low-voltage detection reset (option) has occurred.</li> <li>Otherwise, the bit retains the value existing before the reset occurred.</li> <li>The low-voltage detection reset function is provided for specific models.</li> <li>Read access to this bit sets it to "0".</li> <li>The bit is read-only. Any value written is meaningless.</li> </ul>
bit1	HWR: Hardware reset flag bit	<ul> <li>This bit is set to "1" to indicate that a reset other than software resets has occurred. When any of bits 2 to 5 is set to "1", therefore, this bit is set to "1" as well.</li> <li>Otherwise, the bit retains the value existing before the reset occurred.</li> <li>Read access to this bit sets it to "0".</li> <li>The bit is read-only. Any value written is meaningless.</li> </ul>
bit0	SWR: Software reset flag bit	<ul> <li>This bit is set to "1" to indicate that a software reset has occurred.</li> <li>Otherwise, the bit retains the value existing before the reset occurred.</li> <li>Read access to this bit or a power-on reset sets it to "0".</li> <li>The bit is read-only. Any value written is meaningless.</li> </ul>

Table 7.2-1 Functions of Bits in Reset Source Register (RSRR)

Note:

Reading the reset source register clears its contents. To use the reset source register for calculation, therefore, you should move the contents of the register to RAM in advance.

CHAPTER 7 RESET

# CHAPTER 8 INTERRUPTS

This chapter explains the interrupts.

8.1 Interrupts

### 8.1 Interrupts

### This section explains the interrupts.

### Overview of Interrupts

The  $F^2MC$ -8FX family has 24 interrupt request input lines corresponding to peripheral resources, for each of which an interrupt level can be set independently.

When a peripheral resource generates an interrupt request, the interrupt request is output to the interrupt controller. The interrupt controller checks the interrupt level of that interrupt request and then passes the occurrence of the interrupt to the CPU. The CPU services the interrupt according to the interrupt acceptance status. Interrupt requests also release the device from standby mode to resume instruction execution.

### Interrupt Requests from Peripheral Resources

Figure 8.1-1 lists the interrupt requests corresponding to peripheral resources. When an interrupt is accepted, a branch to the interrupt service routine takes place with the content of the interrupt vector table address corresponding to the interrupt request as the address of the branch destination.

The priority for each interrupt request can be set to one of four levels using the interrupt level setting registers (ILR0 to ILR5).

If another interrupt request with the same or lower level occurs during execution of the interrupt service routine, the interrupt is processed after the current interrupt handler routine completes. If interrupt requests of the same level occur at the same time, IRQ0 is assigned the highest priority.

	Vector Tab	le Address	Bit in Interrupt Level	Priority for Equal-level Interrupt	
Interrupt Request	Upper	Lower	Setting Register	Requests (Generated Simultaneously)	
IRQ0	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1:0]	Highest	
IRQ1	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]		
IRQ2	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1:0]	1 <b>T</b>	
IRQ3	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1:0]		
IRQ4	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]		
IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]		
IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1:0]		
IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1:0]		
IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1:0]		
IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]		
IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1:0]		
IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1:0]		
IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]		
IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	1	
IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1:0]		
IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1:0]		
IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]		
IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]		
IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1:0]		
IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]		
IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	1	
IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]		
IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1:0]	] ▼	
IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1:0]	Lowest	

### Table 8.1-1 Interrupt Requests and Interrupt Vectors

For interrupt sources, see "APPENDIX B Table of Interrupt Causes".

# 8.1.1 Interrupt Level Setting Registers (ILR0 to ILR5)

The interrupt level setting registers (ILR0 to ILR5) contain 24 pairs of bits assigned for the interrupt requests from different peripheral resources. Each pair of bits (interrupt level setting bits as two-bit data) sets each interrupt level.

### ■ Configuration of Interrupt Level Setting Registers (ILR0 to ILR5)

Register	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ILR0	00079 <sub>H</sub>	L03	[1:0]	L02	[1:0]	L01	[1:0]	L00	[1:0]	R/W 11111111 <sub>B</sub>
										1
ILR1	0007A <sub>H</sub>	L07	[1:0]	L06	[1:0]	L05	[1:0]	L04	[1:0]	R/W 11111111 <sub>B</sub>
										-
ILR2	0007B <sub>H</sub>	L11	[1:0]	L10	[1:0]	L09	[1:0]	L08	[1:0]	R/W 11111111 <sub>B</sub>
										-
ILR3	0007C <sub>H</sub>	L15	[1:0]	L14	[1:0]	L13	[1:0]	L12	[1:0]	R/W 11111111 <sub>B</sub>
										-
ILR4	0007D <sub>H</sub>	L19	[1:0]	L18	[1:0]	L17	[1:0]	L16	[1:0]	R/W 11111111 <sub>B</sub>
										-
ILR5	0007E <sub>H</sub>	L23	[1:0]	L22	[1:0]	L21	[1:0]	L20	[1:0]	R/W 11111111 <sub>B</sub>

### Figure 8.1-1 Configuration of Interrupt Level Setting Registers

The interrupt level setting registers assign each pair of bits for a different interrupt request. The values of interrupt level setting bits in these registers specify interrupt service priorities (interrupt levels 0 to 3).

The interrupt level setting bits are compared with the interrupt level bits in the condition code register (CCR: IL1, IL0).

When interrupt level 3 is set for an interrupt request, the CPU ignores the interrupt request.

Table 8.1-2 shows the relationships between interrupt level setting bits and interrupt levels.

Table 8.1-2 Relationships Between Interrupt Level Setting Bits and Interrupt Levels

LXX	LXX	Interrupt Level	Priority
0	0	0	Highest
0	1	1	<b>▲</b>
1	0	2	▼
1	1	3	Lowest (No interrupt accepted)

XX:0 to 23 Corresponding interrupt number

During execution of a main program, usually, the interrupt level bits in the condition code register (CCR: IL1, IL0) contain " $11_B$ ".
# 8.1.2 Interrupt Processing

When an interrupt request is generated by a peripheral resource, the interrupt controller passes the interrupt level to the CPU. When the CPU is ready to accept interrupts, it temporarily halts the program currently being executed and executes an interrupt service routine.

#### Interrupt Processing

The procedure of processing an interrupt takes the following steps: the generation of an interrupt resource in a peripheral resource, the execution of the main program, the setting of the interrupt request flag bit, the evaluation of the interrupt request enable bit, the evaluation of interrupt level (ILR0 to ILR5 and CCR:IL1, IL0), the checking for any equal-level interrupt request, and the evaluation of the interrupt enable flag (CCR:I).

Figure 8.1-2 illustrates the steps to take for interrupt processing.

Figure 8.1-2 Interrupt Processing Steps



- (1) Any interrupt request is disabled immediately after a reset. In the peripheral resource initialization program, initialize those peripheral resources which generate interrupts and set their interrupt levels in their respective interrupt level setting registers (ILR0 to ILR5) before starting operating the peripheral resources. The interrupt level can be set to 0, 1, 2, or 3. Level 0 is given the highest priority, and level 1 the second highest. Setting level 3 for a peripheral resource disables interrupts from that resource.
- (2) Execute the main program (or the interrupt service routine for nested interrupts).
- (3) When an interrupt is triggered in a peripheral resource, the interrupt request flag bit of the peripheral resource is set to "1". If the interrupt request enable bit of the peripheral resource has been set to enable interrupts, the interrupt request is then output to the interrupt controller.
- (4) The interrupt controller always monitors interrupt requests from individual peripheral resources and transfers the highest-priority interrupt level, to the CPU, among the interrupt levels of the currently generated interrupt requests. The relative priority to be assigned if another request with the same interrupt level occurs simultaneously is also determined at this time.
- (5) If the received interrupt level or priority is lower than the level set in the interrupt level bits in the condition code register (CCR: IL1, IL0), the CPU checks the content of the interrupt enable flag (CCR:I) and, if interrupts are enabled (CCR:I = 1), accepts the interrupt.
- (6) The CPU pushes the contents of the program counter (PC) and program status (PS) register onto the stack, fetches the start address of the interrupt service routine from the corresponding interrupt vector table, changes the value of the interrupt level bits in the condition code register (CCR: IL1, IL0) to the value of the received interrupt level, then starts the execution of the interrupt service routine.
- (7) Finally, the CPU uses the RETI instruction to restore the program counter (PC) and program status (PS) values from the stack and resumes execution from the instruction that follows the instruction executed prior to the interrupt.

Note:

The interrupt request flag bits of peripheral resources are not automatically cleared to "0" after an interrupt request is accepted. The bits must therefore be cleared to "0" by a program (by writing "0" to the interrupt request flag bit) in the interrupt service routine.

An interrupt causes the device to recover from standby mode (low power consumption mode). For details, see "6.8 Operations in Low-power Consumption Modes (Standby Modes)".

## 8.1.3 Nested Interrupts

You can set different interrupt levels for two or more interrupt requests from peripheral resources in the interrupt level setting registers (ILR0 to ILR5) to process the nested interrupts.

#### Nested Interrupts

If an interrupt request of higher-priority interrupt level occurs while an interrupt service routine is being executed, the CPU halts processing of the current interrupt and accepts the higher-priority interrupt request. The interrupt level can be set to 0 to 3. If it is set to 3, the CPU will accept no interrupt request.

#### [Example: Nested interrupts]

To assign higher priority to external interrupts over timer interrupts as an example of processing nestedinterrupts, set the timer interrupt and external interrupt levels to 2 and 1, respectively. If an external interrupt occurs while a timer interrupt is being processed with these settings in use, the interrupts are processed as shown in Figure 8.1-3.



Figure 8.1-3 Example of Processing Nested Interrupts

- While a timer interrupt is being processed, the interrupt level bits in the condition code register (CCR: IL1, IL0) hold the same value as that of the interrupt level setting registers (ILR0 to ILR5) corresponding to the current timer interrupt (level 2 in this example). If an interrupt request with a higher-priority interrupt level (level 1 in the example) occurs, the higher-priority interrupt is processed preferentially.
- To temporarily disable nested interrupt processing while a timer interrupt is being processed, set the interrupt enable flag in the condition code register to disable interrupts (CCR:I = 0) or set the interrupt level bits (CCR: IL1, IL0) to " $00_B$ ".
- Executing the interrupt return instruction (RETI) after interrupt processing is completed restores the program counter (PC) and program status (PS) values saved in a stack and resumes the processing of the interrupted program. Restoring the program status (PS) also restores the condition code register (CCR) to its value existing prior to the interrupt.

# 8.1.4 Interrupt Processing Time

The time between an interrupt request being generated and control being passed to the interrupt processing routine is equal to the sum of the time until the currently executing instruction completes and the interrupt handling time (time required to initiate interrupt processing). This time consists of a maximum of 26 machine clock cycles.

#### Interrupt Processing Time

The interrupt request sampling wait time and interrupt handling time intervene between the occurrence and acceptance of an interrupt request and the execution of the relevant interrupt service routine.

#### Interrupt request sampling wait time

Whether an interrupt request has occurred is determined through the sampling of the interrupt request during the last cycle of each instruction. The CPU cannot therefore recognize interrupt requests during the execution of each instruction. The maximum length of this delay occurs if the interrupt request is generated immediately after the DIVU instruction requiring the longest instruction cycle (17 machine clock cycles) starts executing.

#### Interrupt handling time

After receiving an interrupt, the CPU requires 9 machine clock cycles to perform the following interrupt processing setup:

- Saves the program counter (PC) and program status (PS) values.
- Sets the PC to the start address (interrupt vector) of interrupt service routine.
- Updates the interrupt level bits (PS:CCR:IL1, IL0) in the program status (PS) register.



#### Figure 8.1-4 Interrupt Processing Time

When an interrupt request is generated immediately after the beginning of execution of the DIVU instruction requiring the longest execution cycle (17 machine clock cycles), it takes an interrupt processing time of 17+9=26 machine clock cycles.

The machine clock changes depending on the clock mode and main clock speed switching (gear function). For details, refer to "CHAPTER 6 CLOCK CONTROLLER".

# 8.1.5 Stack Operations During Interrupt Processing

# This section describes how registers are saved and restored during interrupt processing.

#### Stack Operation at the Start of Interrupt Processing

Once the CPU accepts an interrupt, it automatically saves the current program counter (PC) and program status (PS) values onto a stack.

Figure 8.1-5 shows how the stack is used at the start of interrupt processing.





#### Stack Operation upon Returning from Interrupt

When the interrupt return instruction (RETI) is executed to end interrupt processing, the program status (PS) and then the program counter (PC) are restored from the stack, in the reverse order from which they were saved to the stack when interrupt processing started. This restores the PS and PC values to their states prior to starting interrupt processing.

Note:

As the accumulator (A) and temporary accumulator (T) are not saved onto the stack automatically, use the PUSHW and POPW instructions to save and restore the A and T values.

# 8.1.6 Interrupt Processing Stack Area

# The stack area in RAM is used for interrupt processing. The stack pointer (SP) contains the start address of the stack area.

#### ■ Interrupt Processing Stack Area

The stack area is also used to save and restore the program counter (PC) when subroutine call (CALL) or vector call (CALLV) instructions are executed and to temporarily save and restore the registers via the PUSHW and POPW instructions.

- The stack area is located in RAM together with the data area.
- It is advisable to initialize the stack pointer (SP) to the maximum RAM address and allocate data areas starting from the minimum RAM address.

Figure 8.1-6 shows an example of setting the stack area.





#### Note:

The stack area is allocated in descending order of addresses for interrupts, subroutine calls, and the PUSHW instruction; it is deallocated in ascending order of addresses for return (PETI, RET) and POPW instructions. When the stack area address used decreases for nested interrupts or subroutines, prevent the stack area from overlapping the data area or general-purpose register area containing other data.

# CHAPTER 9 I/O PORT

This chapter describes the functions and operations of the I/O ports.

- 9.1 Overview of I/O Ports
- 9.2 Port 0
- 9.3 Port 1
- 9.4 Port F
- 9.5 Port G

# 9.1 Overview of I/O Ports

#### I/O ports are used to control general-purpose I/O pins.

#### Overview of I/O Ports

The I/O port has functions to output data from the CPU and load inputted signals into the CPU, via the port data register (PDR). It is also possible to set the input/output direction of the I/O pins as desired at the bit level, via the port direction register (DDR).

Table 9.1-1 lists the registers for each port.

#### Table 9.1-1 Each Port Registers

Register name		Read/Write	Initial value
Port 0 data register	(PDR0)	R, RM/W	00000000 <sub>B</sub>
Port 0 direction register	(DDR0)	R/W	00000000 <sub>B</sub>
Port 1 data register	(PDR1)	R, RM/W	00000000 <sub>B</sub>
Port 1 direction register	(DDR1)	R/W	00000000 <sub>B</sub>
Port F data register	(PDRF)	R, RM/W	00000000 <sub>B</sub>
Port F direction register	(DDRF)	R/W	00000000 <sub>B</sub>
Port G data register	(PDRG)	R, RM/W	00000000 <sub>B</sub>
Port G direction register	(DDRG)	R/W	00000000 <sub>B</sub>
Port 0 pull-up register	(PUL0)	R/W	00000000 <sub>B</sub>
Port 1 pull-up register	(PUL1)	R/W	00000000 <sub>B</sub>
Port G pull-up register	(PULG)	R/W	00000000 <sub>B</sub>
A/D input disable register lower	(AIDRL)	R/W	00000000 <sub>B</sub>
Input level selection register	(ILSR)	R/W	00000000 <sub>B</sub>
Input level selection register 2*	(ILSR2)	R/W	00000000 <sub>B</sub>

R/W: Readable/writable (Read value is the same as the write value.)

R, RM/W: Readable/writable (Read value is different from write value, write value is read by read-modify-write instruction.)

\*: Only for 5V products, it is an effective register.

# 9.2 Port 0

#### Port 0 is a general-purpose I/O port.

This section focuses on functions as a general-purpose I/O port. See the chapters on each peripheral function for details about peripheral functions.

#### ■ Port 0 Configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Input level selection register 2 (ILSR2)

#### Port 0 Pins

Port 0 has eight I/O pins. Table 9.2-1 lists the port 0 pins.

#### Table 9.2-1 Port 0 Pins

Din name	Function	Shared peripheral functions	I/O type			
Finname	Function	Shared peripheral functions	Input*	Output	OD	PU
		AN00 analog input	Hysteresis/			
P00/IN100/ P00/PPG00	P00 general-purpose I/O	INT00 external interrupt input	Analog/	CMOS	-	0
100/11000		8/16-bit PPG0 ch.0 output	Automotive			
		AN01 analog input	Hysteresis/			
P01/IN101/ AN01/PPG01	P01 general-purpose I/O	INT01 external interrupt input	Analog/	CMOS	-	Ο
71101/11 001		8/16-bit PPG0 ch.1 output	Automotive			
		AN02 analog input	Hysteresis/			
P02/IN102 AN02/SCK	P02 general-purpose I/O	INT02 external interrupt input	Analog/	CMOS	-	0
ANUZ/BEK		LIN-UART clock I/O	Automotive			
	P03 general-purpose I/O	AN03 analog input	Hysteresis/	CMOS		0
P03/IN103/		INT03 external interrupt input	Analog/		-	
11105/501		LIN-UART data output	Automotive			
		AN04 analog input	Hysteresis/			
P04/IN104/ AN04/SIN	P04 general-purpose I/O	INT04 external interrupt input	Analog/	CMOS	-	Ο
AINO-7/SIIN		LIN-UART data input	Automotive			
		AN05 analog input	<b>TT</b> /			
P05/INT05/	PO5 general-nurnose I/O	INT05 external interrupt input	Hysteresis/	CMOS	_	$\circ$
AN05/TO00	1 05 general purpose 1/0	8/16-bit compound timer0	Automotive	CINOS		)
		ch.0 output				
		AN06 analog input	Hysteresis/			
P06/INT06/	P06 general-purpose I/O	INT06 external interrupt input	Analog/	CMOS	-	0
AN06/1'001	2 00 Sellerar Parkose 1.0	8/16-bit compound timer0 ch.1 output	Automotive			
P07/INT07/		AN07 analog input	Hysteresis/			
AN07	P07 general-purpose I/O	INT07 external interrupt input	Analog/ Automotive	CMOS	-	0

OD: Open drain, PU: Pull-up

\*: For 5V products, the hysteresis input can be switched to an automotive input. It becomes a hysteresis input besides.

#### ■ Block Diagram of Port 0



#### Figure 9.2-1 Block Diagram of Port 0

# 9.2.1 Port 0 Registers

#### This section describes the port 0 registers.

#### ■ Port 0 Register Function

Table 9.2-2 lists the port 0 register functions.

#### Table 9.2-2 Port 0 Register Function

Register name	Data	Read	Write					
PDRO	0	Pin state is "L" level.	PDR register value is "0".	As output port, outputs "L" level.				
I DK0	1	Pin state is "H" level.	PDR register value is "1".	As output port, outputs "H" level.				
	0		Port input enabled					
DDR0	1		Port output enabled					
	0		Pull-up disabled					
FULU	1		Pull-up enabled					
	0		Analog input enabled					
AIDKL	1	Port input enabled						
н ср	0		Hysteresis input level select	ction				
ILSK	1	CMOS input level selection						
П СР.2*	0		Hysteresis input level selection					
ILSK2	1	Automotive input level selection						

\*: Only for 5V products, it is an effective register.

Table 9.2-3 lists the correspondence between port 0 pins and each register bit.

Table 9.2-3 Correspondence between Registers and Pins for Port 0

	Correspondence between related register bits and pins								
Pin name	P07	P06	P05	P04	P03	P02	P01	P00	
PDR0									
DDR0	hit7	hit6	hit5	hit/	hit?	hit?	hit1	h;t()	
PUL0	UII /	0110	011.5	0114	0115	0112	UIU	bito	
AIDRL									
ILSR	-	-	-	bit2	-	-	-	-	
ILSR2*	bit0								

\*: Only for 5V products, it is an effective register.

# 9.2.2 Operations of Port 0

#### This section describes the operations of port 0.

#### Operations of Port 0

- Operation as an output port
  - Setting the corresponding DDR register bit to "1" sets a pin as an output port.
  - When a pin is set as an output port, it outputs the value of the PDR register to pins.
  - If data is written to the PDR register, the value is stored in the output latch and output to the pin as it is.
  - Reading the PDR register returns the PDR register value.

#### • Operation as an input port

- Setting the corresponding DDR register bit to "0" sets a pin as an input port.
- When using the analog input shared pin as an input port, set the corresponding bits in the A/D input disable register low (AIDRL) to "1".
- If data is written to the PDR register, the value is stored in the output latch but not output to the pin.
- Reading the PDR register returns the pin value. However, the read-modify-write command returns the PDR register value.

• Operation as a peripheral function output

- Setting the output enable bit of a peripheral function sets the corresponding pin as a peripheral function output.
- The pin value can be read from the PDR register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on PDR register. However, the read-modify-write command returns the PDR register value.
- Operation as a peripheral function input
  - Set the DDR register bit, which is corresponding to the peripheral function input pin, to "0" to set a pin as an input port.
  - As with an input port, when using the analog input shared pin as another peripheral function input, configure it as an input port.
  - Reading the PDR register returns the pin value, regardless of whether the peripheral function uses an input pin. However, the read-modify-write command returns the PDR register value.

Operation at reset

• Resetting the CPU initializes the DDR register values to "0", and sets the port input enabled. Note that the pin sharing for the analog input is set its port input disabled since A/D input disable register low (AIDRL) is initialized to "0".

- Operation in stop mode and watch mode
  - If the pin state specification bit in the standby control register (STBC:SPL) is set to "1" when the device switches to stop or watch mode, the pin is set forcibly to the high-impedance state regardless of the DDR register value. Note that the input is locked to "L" and blocked in order to prevent leaks due to freed input. However, if the interrupt input is enabled for the external interrupt control register (EIC) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the external interrupt selection circuit, the input is enabled and not blocked.
  - If the pin state specification bit is "0", the state remains in port I/O or peripheral function I/O and the output is maintained.
- Operation as an analog input
  - Set the DDR register bit, which is corresponding to the analog input pin, to "0", and set the AIDRL register bit to "0".
  - Set the corresponding PUL register bit to "0".
- Operation of the external interrupt input pin
  - Set the DDR register bit, which is corresponding to the external interrupt input pin, to "0".
  - Pin values are continuously input to the external interrupt circuit. When using the pin for a function other than an interrupt, you must disable the corresponding external interrupt.
- Operation of the pull-up control register
  - Writing "1" to the PUL register internally connects the pull-up resistor to the pin. When the output is "L" level, the pull-up resistor is disconnected regardless of the PUL register value.
- Operation of the input level selection register 2
  - The ILSR2 register is a valid register only for 5V models.
  - Setting bit 0 of the ILSR2 register to "1" changes the port 0 input level from the hysteresis input level to the automotive input level. The hysteresis input level is used when bit 0 of the ILSR2 register is "0".
  - Only modify the port 0 input level setting when the peripheral functions input are halted.
  - Table 9.2-4 shows the pin states of the port.

Table 9.2-4 Pin State of Port 0

Operating state	Normal operation Sleep Stop (SPL=0) Watch (SPL=0)	Stop (SPL=1) Watch (SPL=1)	At reset
Pin state	I/O port/ peripheral function I/O	Hi-Z (the pull-up setting is enabled) Input cutoff (If external interrupts are enabled, the external interrupt can be input.)	Hi-Z Input disabled*

SPL: Pin state specification bit in standby control register (STBC:SPL)

Hi-Z: High impedance

\*: "Input disabled" means the state that the operation of the input gate close to the pin is disabled.

# 9.3 Port 1

#### Port 1 is a general-purpose I/O port.

This section focuses on functions as a general-purpose I/O port. See the chapters on each peripheral function for details about peripheral functions.

#### Port 1 Configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up control register (PUL1)
- Input level selection register (ILSR)
- Input level selection register 2 (ILSR2)

#### Port 1 Pins

Port 1 has seven I/O pins.

Table 9.3-1 lists the port 1 pins.

Table	9.3-1	Port 1	Pins
-------	-------	--------	------

Pin name	Eunction	Shared peripheral functions	I/O type			
Finnanie	T diretion		Input*	Output	OD	PU
P10/UI0	P10 general-purpose I/O	UI0 UART/SIO ch.0 data input	Hysteresis/CMOS/ Automotive	CMOS	-	0
P11/UO0	P11 general-purpose I/O	UO0 UART/SIO ch.0 data output	Hysteresis/Automotive	CMOS	-	0
P12/ UCK0/EC0	P12 general-purpose I/O	UO0 UART/SIO ch.0 clock I/O		CMOS		
		EC0 8/16-bit composite timer ch.0 clock input	Hysteresis/Automotive		-	0
P13/	P12 gaparal purposa I/O	TRG0 16-bit PPG ch.0 trigger input	Hystoresis/Automotive	CMOS		0
TRG0/ADTG	P15 general-purpose I/O	ADTG A/D trigger activation input	Trysteresis/Automotive	CMOS	-	
P14/PPG0	P14 general-purpose I/O	PPG0 16-bit PPG ch.0 output	Hysteresis/Automotive	CMOS	-	Ο
P15	P15 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	Ο
P16	P16 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	Ο

OD: Open drain, PU: Pull-up

\*: For 5V products, the hysteresis input can be switched to the automotive input. It becomes hysteresis input or CMOS input besides.

#### ■ Block Diagram of Port 1



Figure 9.3-1 Block Diagram of Port 1

# 9.3.1 Port 1 Registers

#### This section describes the port 1 registers.

#### ■ Port 1 Register Function

Table 9.3-2 lists the port 1 register functions.

#### Table 9.3-2 Port 1 Register Function

Register name	Data	Read Read read-modify-write		Write			
	0	Pin state is "L" level.	PDR register value is "0".	As output port, outputs "L" level.			
TDRI	1	Pin state is "H" level.	PDR register value is "1".	As output port, outputs "H" level.			
	0		Port input enabled				
DDRI	1	Port output enabled					
	0		Pull-up disabled				
FULI	1		Pull-up enabled				
ПСР	0		Hysteresis input level sele	ction			
ILSK	1	CMOS input level selection					
II SP2*	0		Hysteresis input level selection				
ILSK2*	1	Automotive input level selection					

\*: Only for 5V products, it is an effective register.

Table 9.3-3 lists the correspondence between port 1 pins and each register bit.

Table 9.3-3	Correspondence	between Registers	and Pins for Port 1
-------------	----------------	-------------------	---------------------

		Correspondence between related register bits and pins							
Pin name	-	P16	P15	P14	P13	P12	P11	P10	
PDR1									
DDR1	-	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
PUL1									
ILSR	-	-	-	-	-	-	-	bit0	
ILSR2*	-	-	bit1						

\*: Only for 5V products, it is an effective register.

# 9.3.2 Operations of Port 1

#### This section describes the operations of port 1.

#### Operations of Port 1

- Operation as an output port
  - Setting the corresponding DDR register bit to "1" sets a pin as an output port.
  - For a peripheral function sharing pins, disable its output.
  - When a pin is set as an output port, it outputs the value of the PDR register to pins.
  - If data is written to the PDR register, the value is stored in the output latch and output to the pin as it is.
  - Reading the PDR register returns the PDR register value.

#### • Operation as an input port

- Setting the corresponding DDR register bit to "0" sets a pin as an input port.
- For a peripheral function sharing pins, disable its output.
- If data is written to the PDR register, the value is stored in the output latch but not output to the pin.
- Reading the PDR register returns the pin value. However, the read-modify-write command returns the PDR register value.

Operation as a peripheral function output

- Setting the output enable bit of a peripheral function sets the corresponding pin as a peripheral function output.
- The pin value can be read from the PDR register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on PDR register. However, the read-modify-write command returns the PDR register value.
- Operation as a peripheral function input
  - Set the DDR register bit, which is corresponding to the peripheral function input pin, to "0" to set a pin as an input port.
  - Reading the PDR register returns the pin value, regardless of whether the peripheral function uses an input pin. However, the read-modify-write command returns the PDR register value.
- Operation at reset
  - Resetting the CPU initializes the DDR register values to "0", and sets the port input enabled.

- Operation in stop mode and watch mode
  - If the pin state specification bit in the standby control register (STBC:SPL) is set to "1" when the device switches to stop or watch mode, the pin is set forcibly to the high-impedance state regardless of the DDR register value. Note that the input is locked to "L" and blocked in order to prevent leaks due to freed input. However, if the interrupt input of P10/U10, P12/U0K0, P13/TRG0/ADTG port is enabled for the external interrupt control register (EIC) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the external interrupt selection circuit, the input is enabled and not blocked.
  - If the pin state specification bit is "0", the state remains in port I/O or peripheral function I/O and the output is maintained.
- Operation of the pull-up control register
  - Writing "1" to the PUL register internally connects the pull-up resistor to the pin. When the output is "L" level, the pull-up resistor is disconnected regardless of the PUL register value.
- Operation of the input level selection register
  - Setting "1" to the bit0 of ILSR register changes only P10 from the hysteresis input level to the CMOS input level. When the bit0 of ILSR register is "0", it should be the hysteresis input level.
  - For pins other than P10, the CMOS input level cannot be selected; however, only the hysteresis input level or the automotive input level can.
  - Make sure that the input level for P10 is changed during the peripheral function (UART/SIO) stopped.

• Operation of the input level selection register 2

- The ILSR2 register is a valid register only for 5V models.
- Setting bit 1 of the ILSR2 register to "1" changes the port 1 input level from the hysteresis input level to the automotive input level. The hysteresis input level is used when bit 1 of the ILSR2 register is "0".
- P10 only uses the automotive input level when bit 0 of the ILSR register is "0". In the case of P10 only, setting "1" to bit 0 of the ILSR register has priority over ILSR2.
- Only modify the port 1 input level setting when the peripheral functions (ART/SIO) are halted.

Table 9.3-4 shows the pin states of the port.

#### Table 9.3-4 Pin State of Port 1

Operating state	Normal operation Sleep Stop (SPL=0) Watch (SPL=0)	Stop (SPL=1) Watch (SPL=1)	At reset
Pin state	I/O port/ peripheral function I/O	Hi-Z (the pull-up setting is enabled) Input cutoff	Hi-Z Input enabled* (Not functional)

SPL: Pin state specification bit in standby control register (STBC:SPL)

Hi-Z: High impedance

\*: "Input enabled" means that the input function is enabled; it requires the pull-up or pull-down operation, or preventing leaks by external inputs. Same as other ports when used as an output port.

# 9.4 Port F

#### Port F is a general-purpose I/O port.

This section focuses on functions as a general-purpose I/O port. See the chapters on each peripheral function for details about peripheral functions.

#### ■ Port F Configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)
- Input level selection register 2 (ILSR2)

#### Port F Pins

Port F has two I/O pins.

Table 9.4-1 lists the port F pins.

#### Table 9.4-1 Port F Pins

Pin name	Function	Sharad paripharal functions	I/O type			
	Function		Input*	Output	OD	PU
PF0	PF0 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	-
PF1	PF1 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	-

OD: Open drain, PU: Pull-up

\*: For 5V products, the hysteresis input can be switched to the automotive input. It becomes hysteresis input besides.

# ■ Block Diagram of Port F



Figure 9.4-1 Block Diagram of Port F

# 9.4.1 Port F Registers

#### This section describes the port F registers.

#### ■ Port F Register Function

Table 9.4-2 lists the port F register functions.

#### Table 9.4-2 Port F Register Function

Register name	Data	Read	Write						
PDPF	0	Pin state is "L" level.	PDR register value is "0".	As output port, outputs "L" level.					
I DKI*	1	Pin state is "H" level.	PDR register value is "1".	As output port, outputs "H" level.					
DDRE	0		Port input enabled						
DDRI	1	Port output enabled							
II SP2*	0	Hysteresis input level selection							
ILSK2	1	Automotive input level selection							

\*: Only for 5V products, it is an effective register.

Table 9.4-3 lists the correspondence between port F pins and each register bit.

#### Table 9.4-3 Correspondence Between Registers and Pins for Port F

		Correspondence between related register bits and pins									
Pin name	-	PF1 PF0									
PDRF							bit1	bit0			
DDRF	-	-	-	-	-	-	UIU	Dito			
ILSR2*		bit12									

\*: Only for 5V products, it is an effective register.

# 9.4.2 Operations of Port F

#### This section describes the operations of port F.

#### Operations of Port F

- Operation as an output port
  - Setting the corresponding DDR register bit to "1" sets a pin as an output port.
  - For a peripheral function sharing pins, disable its output.
  - When a pin is set as an output port, it outputs the value of the PDR register to pins.
  - If data is written to the PDR register, the value is stored in the output latch and output to the pin as it is.
  - Reading the PDR register returns the PDR register value.
- Operation as an input port
  - Setting the corresponding DDR register bit to "0" sets a pin as an input port.
  - If data is written to the PDR register, the value is stored in the output latch but not output to the pin.
  - Reading the PDR register returns the pin value. However, the read-modify-write command returns the PDR register value.
- Operation at reset
  - Resetting the CPU initializes the DDR register values to "0", and sets the port input enabled.
- Operation in stop mode and watch mode
  - If the pin state specification bit in the standby control register (STBC:SPL) is set to "1" when the device switches to stop or watch mode, the pin is set forcibly to the high-impedance state regardless of the DDR register value. Note that the input is locked to "L" and blocked in order to prevent leaks due to freed input.
  - If the pin state specification bit is "0", the state remains in port I/O and the output is maintained.
- Operation of the input level selection register 2
  - The ILSR2 register is a valid register only for 5V models.
  - Setting bit 2 of the ILSR2 register to "1" changes the port F input level from the hysteresis input level to the automotive input level. The hysteresis input level is used when bit 2 of the ILSR2 register is "0".

Table 9.4-4 shows the pin states of the port.

Table 9.4-4 Pin State of Port F

Operating state	Normal operation Sleep Stop (SPL=0) Watch (SPL=0)	Stop (SPL=1) Watch (SPL=1)	At reset
Pin state	I/O port	Hi-Z Input cutoff	Hi-Z Input enabled* (Not functional)

SPL: Pin state specification bit in standby control register (STBC:SPL)

Hi-Z: High impedance

\*: "Input enabled" means that the input function is enabled; it requires the pull-up or pull-down operation, or preventing leaks by external inputs. Same as other ports when used as an output port.

# 9.5 Port G

#### Port G is a general-purpose I/O port.

This section focuses on functions as a general-purpose I/O port.

#### Port G Configuration

Port G is made up of the following elements.

- General-purpose I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up control register (PULG)
- Input level selection register 2 (ILSR2)

#### Port G Pins

Port G has three I/O pins.

Table 9.5-1 lists the port G pins.

Din nomo	Function	Sharad parinharal functions	I/O type				
Fill Hame	Function	Shared peripheral functions	Input* <sup>3</sup>	Output	OD	PU	
PG0*1	PG0 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	0	
PG1* <sup>2</sup>	PG1 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	0	
PG2* <sup>2</sup>	PG2 general-purpose I/O	Not shared	Hysteresis/Automotive	CMOS	-	0	

OD: Open drain, PU: Pull-up

\*1: For the 5V product, the C pin is used.

\*2: For the single system product, the general-purpose port is used; for the dual system, the sub clock oscillation pin is used.

\*3: For 5V products, the hysteresis input can be switched to an automotive input. It becomes a hysteresis input besides.

# ■ Block Diagram of Port G



Figure 9.5-1 Block Diagram of Port G

# 9.5.1 Port G Registers

#### This section describes the port G registers.

#### Port G Register Function

Table 9.5-2 lists the port G register functions.

#### Table 9.5-2 Port G Register Function

Register name	Data	Read	Write						
PDPG	0	Pin state is "L" level.	PDR register value is "0".	As output port, outputs "L" level.					
I DKO	1	Pin state is "H" level.	PDR register value is "1".	As output port, outputs "H" level.					
DDRG	0		Port input enabled						
DDKO	1 Port output enabled								
	0		Pull-up disabled						
FOLG	1	Pull-up enabled							
II SP2*	0	Hysteresis input level selection							
ILSR2	1	Automotive input level selection							

\*: Only for 5V products, it is an effective register.

Table 9.5-3 lists the correspondence between port G pins and each register bit.

#### Table 9.5-3 Correspondence between Registers and Pins for Port G

		Correspondence between related register bits and pins									
Pin name	-	-	PG2 PG1 F								
PDRG											
DDRG	-	-	-	-	-	bit2	bit1	bit0			
PULG											
ILSR2*	-	-	-	-	-	bit6					

\*: Only for 5V products, it is an effective register.

# 9.5.2 Operations of Port G

#### This section describes the operations of port G.

#### Operations of Port G

- Operation as an output port
  - Setting the corresponding DDR register bit to "1" sets a pin as an output port.
  - When a pin is set as an output port, it outputs the value of the PDR register to pins.
  - If data is written to the PDR register, the value is stored in the output latch and output to the pin as it is.
  - Reading the PDR register returns the PDR register value.

#### • Operation as an input port

- Setting the corresponding DDR register bit to "0" sets a pin as an input port.
- If data is written to the PDR register, the value is stored in the output latch but not output to the pin.
- Reading the PDR register returns the pin value. However, the read-modify-write command returns the PDR register value.
- Operation at reset
  - Resetting the CPU initializes the DDR register values to "0", and sets the port input enabled.
- Operation in stop mode and watch mode
  - If the pin state specification bit in the standby control register (STBC:SPL) is set to "1" when the device switches to stop or watch mode, the pin is set forcibly to the high-impedance state regardless of the DDR register value. Note that the input is locked to "L" and blocked in order to prevent leaks due to freed input.
  - If the pin state specification bit is "0", the state remains in port I/O and the output is maintained.
- Operation of the pull-up control register
  - Writing "1" to the PUL register internally connects the pull-up resistor to the pin. When the output is "L" level, the pull-up resistor is disconnected regardless of the PUL register value.
- Operation of the input level selection register 2
  - The ILSR2 register is a valid register only for 5V models.
  - Setting bit 6 of the ILSR2 register to "1" changes the port G input level from the hysteresis input level to the automotive input level. The hysteresis input level is used when bit 6 of the ILSR2 register is "0".

Table 9.5-4 shows the pin states of the port.

Table 9.5-4 Pin State of Port G

Operating state	Normal operation Sleep Stop (SPL=0) Watch (SPL=0)	Stop (SPL=1) Watch (SPL=1)	At reset
Pin state	I/O port	Hi-Z Input cutoff	Hi-Z Input enabled* (Not functional)

SPL: Pin state specification bit in standby control register (STBC:SPL)

Hi-Z: High impedance

\*: "Input enabled" means that the input function is enabled; it requires the pull-up or pull-down operation, or preventing leaks by external inputs. Same as other ports when used as an output port.

#### CHAPTER 9 I/O PORT

# CHAPTER 10 TIMEBASE TIMER

This chapter describes the functions and operations of the timebase timer.

- 10.1 Overview of Timebase Timer
- 10.2 Configuration of Timebase Timer
- 10.3 Registers of the Timebase Timer
- 10.4 Interrupts of Timebase Timer
- 10.5 Explanation of Timebase Timer Operations and Setup Procedure Example
- 10.6 Precautions when Using Timebase Timer

# **10.1** Overview of Timebase Timer

The timebase timer is a 22-bit free-run down-counting counter which is synchronized with the main clock divided by two. The timebase timer has an interval timer function which can repeatedly generate interrupt requests at regular intervals.

#### Interval Timer Function

The interval timer function repeatedly generates interrupt requests at regular intervals by using the main clock divided by two as the count clock.

- The counter of the timebase timer counts down so that an interrupt request is generated every time the selected interval time elapses.
- The interval time can be selected from the following four types.

Table 10.1-1 shows the interval times available to the timebase timer.

#### Table 10.1-1 Interval Times of Timebase Timer

Internal count clock cycle	Interval time			
	$2^{10} \times 2/F_{CH}$ (512.0 µs)			
2/E (0.5 us)	$2^{12} \times 2/F_{CH}$ (2.05ms)			
21 CH (0.5 µs)	$2^{14} \times 2/F_{CH}$ (8.19ms)			
	$2^{16} \times 2/F_{CH}$ (32.77ms)			

F<sub>CH</sub>: Main clock

The values in parentheses represent the values used when the main clock operates at 4MHz.

# **10.2** Configuration of Timebase Timer

The timebase timer consists of the following blocks:

- Timebase timer counter
- Counter clear circuit
- Interval timer selector
- Timebase timer control register (TBTC)

#### Block Diagram of Timebase Timer



#### Figure 10.2-1 Block Diagram of Timebase Timer

#### Timebase timer counter

22-bit down-counter that uses the main clock divided by two as the count clock

#### • Counter clear circuit

This circuit controls clearing of the timebase counter.

#### Interval timer selector

This circuit selects the one bit from four bits in the 22 bits that make up the timebase timer counter to use the interval timer.

#### • Timebase timer control register (TBTC)

This register selects the interval time, clears the counter, controls interrupts and checks the status.

#### Input Clock

The timebase timer uses the main clock divided by two as its input clock (count clock).

#### Output Clock

The timebase timer supplies clocks to the main clock oscillation stabilization wait time timer, the watchdog timer and the prescaler.

# **10.3** Registers of the Timebase Timer

### Figure 10.3-1 shows the register of the timebase timer.

#### ■ Register of the Timebase Timer

Figure 10.3-1 Register of the Timebase Timer									
Timebase time	r control re	gister							
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
000A <sub>H</sub>	TBIF	TBIE	-	-	-	TBC1	TBC0	TCLR	00000000 <sub>B</sub>
	R(RM1),W	R/W	R0/WX	R0/WX	R0/WX	R/W	R/W	R/W	1
R(RM1),W: Re (RI R/W: Re R0/WX: Un R0,W: Wi	adable/wri MW) instru adable/wri idefined bit rite only (W	table (Re ction) table (Re (Read va /ritable, "(	ad value i ad value i alue is "0" )" is read)	s different s the sam , writing h	t from writ le as write as no effe	e value, "′ e value) ect on ope	I" is read⊺ ration)	by read-m	nodify-write

# **10.3.1** Timebase Timer Control Register (TBTC)

The timebase timer control register (TBTC) selects the interval time, clears the counter, controls interrupts and checks the status.

### ■ Timebase Timer Control Register (TBTC)

000AH TBIF TBIE TBC1 TBC0 TCLR 0000000B	
R(RM1),W R/W R0/WX R0/WX R0/WX R/W R/W R0,W	
	1
TCLR Timebase timer initialization bit	
Read Write	
0 "0" is always read No change,	
1 - timebase timer	
	1
Interval time select bit	
(Main clock Fcн = 4MHz)	
0 0 2 <sup>10</sup> x 2/Fcн (512.0 μs)	
0 1 2 <sup>12</sup> х 2/Fсн (2.05 ms)	
1 0 2 <sup>14</sup> х 2/Fсн (8.19 ms)	
1 1 2 <sup>то</sup> х 2/Есн (32.77 ms)	J
TBIE Timebase timer interrupt request enable bit	1
0 Disables output of interrupt request	
1 Enables output of interrupt request	
	1
TBIE Timebase timer interrupt request flag bit	]
Read Write	
0 Interval time has not elapsed Clears bit	
1 Interval time has No change,	1
elapsed No effect on operation	
R(RM1),W : Readable/writable (Read value is different from write value, "1" is read by read-modify-write (RMW)	instruction)
R/W : Readable/writable (Read value is the same as write value)	
RU/VVA : Underined bit (Read value is "0", writing has no effect on operation)	
- : Not used	
: Initial value	

Figure 10.3-2 Timebase Timer Control Register (TBTC)
Bit name		Function					
bit7	TBIF: Timebase timer interrupt request flag bit	Set to "1" when interval time selected by the timebase timer elapses. Interrupt request is outputted when this bit and the timebase timer interrupt request enable bit (TBIE) are set to "1". Writing "0": clears the bit. Writing "1": no effect on the operation. "1" is always read in read-modify-write (RMW) instruction.					
bit6	TBIE: Timebase timer interrupt request enable bit	Enables/disables output of interrupt requests to interrupt controller. <b>Writing ''0'</b> : disables output of timebase timer interrupt requests. <b>Writing ''1'</b> : enables output of timebase timer interrupt requests. Interrupt request is outputted when this bit and the timebase timer interrupt request flag bit (TBIF) are set to "1".					
bit5 to bit3	Unused bits	<ul><li>These bits are unused.</li><li>Read value is always "0".</li><li>Write has no effect on the operation.</li></ul>					
	These bits select interval time.						
		TBC1	TBC0	Interval time select bit (Main clock F <sub>CH</sub> = 4MHz)			
bit2	TBC1, TBC0:	0	0	$2^{10} \times 2/F_{CH}$ (512.0 µs)			
bit1	Interval time select bits	0	1	$2^{12} \times 2/F_{CH}$ (2.05ms)			
		1	0	$2^{14} \times 2/F_{CH}$ (8.19ms)			
		1	1	$2^{16} \times 2/F_{CH}$ (32.77ms)			
bit0	TCLR: Timebase timer initialization bit	<ul> <li>This bit clears the timebase timer counter.</li> <li>Writing "0": ignored and has no effect on the operation.</li> <li>Writing "1": initializes all counter bits to "1".</li> <li>Read value is always "0".</li> <li>Note: When the output of the timebase timer is selected as the count clock for the watchdog timer, using this bit to clear the timebase timer also clears the watchdog timer.</li> </ul>					

#### Table 10.3-1 Functional Description of Each Bit of Timebase Timer Control Register (TBTC)

### **10.4** Interrupts of Timebase Timer

# An interrupt request is triggered when the interval time selected by the timebase timer elapses (interval timer function).

#### Interrupt when Interval Function is in Operation

When the timebase timer counter counts down using the internal count clock and the selected timebase timer counter underflows, the timebase timer interrupt request flag bit (TBTC:TBIF) is set to "1". If the timebase timer interrupt request enable bit is enabled (TBTC:TBIE = 1), an interrupt request (IRQE) will be generated to interrupt controller.

- Regardless of the value of TBIE bit, TBIF bit is set to "1", when the selected bit underflows.
- When TBIF bit is set to "1" and TBIE bit is changed from the disable state to the enable state  $(0 \rightarrow 1)$ , an interrupt request is generated immediately.
- TBIF bit is not set when the counter is cleared (TBTC:TCLR = 1) and the timebase timer counter underflows at the same time.
- Write "1" to TBIF bit to clear an interrupt request in an interrupt processing routine.

Note:

When enabling the output of interrupt requests after canceling a reset (TBTC:TBIE = 1), always clear TBIF bit at the same time (TBTC:TBIF = 0).

Table 10.4-1	Interrupts of	Timebase Timer
--------------	---------------	----------------

Item	Description
Interrupt condition	Interval time set by "TBTC:TBC1" and "TBC0" has elapsed
Interrupt flag	TBTC:TBIF
Interrupt enable	TBTC:TBIE

#### Register and Vector Table for Interrupts of Timebase Timer

Interrupt	Interrupt	Interrupt level	setup register	Vector table address		
source	request No.	Register	Setting bit	Upper	Lower	
Timebase timer	IRQ19	ILR4	L19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	

#### Table 10.4-2 Register and Vector Table for Interrupts of Timebase Timer

Refer to "CHAPTER 8 INTERRUPTS" for the interrupt request numbers and vector tables of all peripheral functions.

#### Note:

If the interval time set for the timebase timer is shorter than the main clock oscillation stabilization wait time, an interrupt request of the timebase timer is generated during the main clock oscillation wait time derived from the transition to the clock mode or standby mode. To prevent this, set the timebase timer interrupt request enable bit of the timebase timer control register (TBTC:TBIE) to "0" to disable interrupts of the timebase timer when entering a mode in which the main clock stops oscillating (stop mode, sub clock mode or sub PLL clock mode).

# 10.5 Explanation of Timebase Timer Operations and Setup Procedure Example

# This section describes the operations of the interval timer function of the timebase timer.

#### Operations of Timebase Timer

The counter of the timebase timer is initialized to " $3FFFF_{H}$ " after a reset and starts counting while being synchronized with the main clock divided by two.

The timebase timer continues to count down as long as the main clock is oscillating. Once the main clock halts, the counter stops counting and is initialized to " $3FFFFF_H$ ".

The settings shown in Figure 10.5-1 are required to use the interval timer function.

		<u> </u>							
Address		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
000A <sub>H</sub>	TBTC	TBIF	TBIE	-	-	-	TBC1	TBC0	TCLR
		0	1				0	۲	0
⊚: Used 1: Set to 0: Set to	bit "1" "0"								

Figure 10.5-1 Settings of Interval Timer Function

When the timebase timer initialization bit in the timebase timer control register (TBTC:TCLR) is set to "1", the counter of the timebase timer is initialized to " $3FFFFF_H$ " and continues to count down. When the selected interval time has elapsed, the timebase timer interrupt request flag bit of the timebase timer control register (TBTC:TBIF) becomes "1". In other words, an interrupt request is generated at each interval time selected, based on the time when the counter was last cleared.

#### Clearing Timebase Timer

If the timebase timer is cleared when the output of the timebase timer is used in other peripheral functions, this will affect the operation by changing the count time or in other manners.

When clearing the counter by using the timebase timer initialization bit (TBTC:TCLR), perform setup so that this does not have unexpected effects on other peripheral functions.

When the output of the timebase timer is selected as the count clock for the watchdog timer, clearing the timebase timer also clears the watchdog timer.

The timebase timer is cleared not only by the timebase timer initialization bit (TBTC:TCLR), but also when the main clock is stopped and a count is required for the oscillation stabilization wait time. More specifically, the timebase timer is cleared in the following situations:

- When moving from the main clock mode or main PLL clock mode to the stop mode
- When moving from the main clock mode or main PLL clock mode to the sub clock mode or sub PLL clock mode
- At power on
- At low-voltage detection reset

The counter of the timebase timer is also cleared and stops the operation if a reset occurs while the main clock is still running after the main clock oscillation stabilization wait time has elapsed. The counter, however, continues to operate during a reset if a count is required for the oscillation stabilization wait time.

#### Operating Examples of Timebase Timer

Figure 10.5-2 shows operating examples of operation under the following conditions:

- 1) When a power-on reset is generated
- 2) When entering the sleep mode during the operation of the interval timer function in the main clock mode or main PLL clock mode
- 3) When entering the stop mode during the main clock mode or main PLL clock mode
- 4) When a request is issued to clear the counter

The same operation is performed when changing to the timebase timer mode as for when changing to the sleep mode.

In the sub clock mode, sub PLL clock mode, main clock mode and main PLL clock mode, the timer operation is stopped during the stop mode, as the timebase timer is cleared and the main clock halts. Upon recovering from the stop mode, the timebase timer is used to count the oscillation stabilization wait time.



#### Figure 10.5-2 Operations of Timebase Timer

## Setup Procedure Example

• Initial Setting

The timebase timer is set up in the following procedure:

1) Disable interrupts.	(TBTC:TBIE = 0)
2) Set the interval time.	(TBTC:TBC1, 0)
3) Enable interrupts.	(TBTC:TBIE = 1)
4) Clear the counter.	(TBTC:TCLR = 1)

• Processing interrupts

1) Clear the interrupt request flag.	(TBTC:TBIF = 0)
2) Clear the counter.	(TBTC:TCLR = 1)

### **10.6** Precautions when Using Timebase Timer

#### Care must be taken for the following points when using the timebase timer.

#### Precautions when Using Timebase Timer

#### • When setting the timer by program

The timer cannot be recovered from interrupt processing, when the timebase timer interrupt request flag bit (TBTC:TBIF) is set to "1" and the interrupt request enable bit is enabled (TBTC:TBIE = 1). Always clear TBIF bit in the interrupt processing routine.

#### Clearing Timebase Timer

The timebase timer is cleared not only by the timebase timer initialization bit (TBTC:TCLR = 1) but also when the oscillation stabilization wait time is required for the main clock. When the timebase timer is selected for the count clock of the watchdog timer (WDTC:CS1, CS0 =  $00_B$  or CS1, CS0, =  $01_B$ ), clearing the timebase timer also clears the watchdog timer.

#### • Peripheral functions receiving clock from timebase timer

In the mode where the source oscillation of the main clock is stopped, the counter is cleared and the timebase timer stops operation. In addition, if the timebase timer is cleared when the output of the timebase timer is used in other peripheral functions, this will affect the operation such as cycle change.

The clock for the watchdog timer is also outputted from the initial state. However, as the watchdog timer counter is cleared at the same time, the watchdog timer operates in the normal cycles.

#### CHAPTER 10 TIMEBASE TIMER

# CHAPTER 11 WATCHDOG TIMER

This chapter describes the functions and operations of the watchdog timer.

- 11.1 Overview of Watchdog Timer
- 11.2 Configuration of Watchdog Timer
- 11.3 Registers of the Watchdog Timer
- 11.4 Explanation of Watchdog Timer Operations and Setup Procedure Example
- 11.5 Precautions when Using Watchdog Timer

# 11.1 Overview of Watchdog Timer

# The watchdog timer serves as a counter used to prevent programs from running out of control.

#### Watchdog Timer Function

The watchdog timer functions as a counter used to prevent programs from running out of control. Once the watchdog timer is activated, its counter needs to be cleared at specified intervals regularly. A watchdog reset is generated if the timer is not cleared within a certain amount of time due to a problem such as the program entering an infinite loop.

The output of either the timebase timer or watch prescaler can be selected as the count clock for the watchdog timer.

The interval times of the watchdog timer are shown in Table 11.1-1. If the counter of the watchdog timer is not cleared, a watchdog reset is generated between the minimum time and the maximum time. Clear the counter of the watchdog timer within the minimum time.

#### Table 11.1-1 Interval Times of Watchdog Timer

Count clock type	Count clock switch bit	Interval time		
oount clock type	(WDTC:CS1, 0)*	Minimum time	Maximum time	
Timebase timer output	00 <sub>B</sub>	524 ms	1.05 s	
(main clock = 4MHz)	01 <sub>B</sub>	262 ms	524 ms	
Watch prescaler output	10 <sub>B</sub>	500 ms	1.00 s	
(sub clock = 32.768 kHz)	11 <sub>B</sub>	250 ms	500 ms	

\*: WDTC:CS1, 0: Count clock switch bit of watchdog timer control register

For information about the minimum and maximum times of the watchdog timer interval, refer to "11.4 Explanation of Watchdog Timer Operations and Setup Procedure Example".

# 11.2 Configuration of Watchdog Timer

The watchdog timer consists of the following blocks:

- Count clock selector
- Watchdog timer counter
- Reset control circuit
- Watchdog timer clear selector
- Counter clear control circuit
- Watchdog timer control register (WDTC)

#### Block Diagram of Watchdog Timer



#### Count clock selector

This selector selects the count clock of the watchdog timer counter.

#### Watchdog timer counter

This is a 1-bit counter that uses the output of either the timebase timer or watch prescaler as the count clock.

#### Reset control circuit

This circuit generates a reset signal when the watchdog timer counter overflows.

#### Watchdog timer clear selector

This selector selects the watchdog timer clear signal.

#### • Counter clear control circuit

This circuit controls the clearing and stopping of the watchdog timer counter.

#### Watchdog timer control register (WDTC)

This register performs setup for activating/clearing the watchdog timer counter as well as for selecting the count clock.

#### Input Clock

The watchdog timer uses the output clock from either the timebase timer or watch prescaler as the input clock (count clock).

# 11.3 Registers of the Watchdog Timer

### Figure 11.3-1 shows the register of the watchdog timer.

		Figure	11.3-1	Register	of The V	Vatchdo	g Timer		
Watchdog tim	er control r	egister (V	VDTC)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
000C <sub>H</sub>	CS1	CS0	-	-	WTE3	WTE2	WTE1	WTE0	00000000 <sub>B</sub>
	R/W	R/W	R0/WX	R0/WX	R0,W	R0,W	R0,W	R0,W	
R/W: R R0/WX: U R0,W: W -: N	eadable/wr ndefined b 'rite only (V ot used	ritable (Re it (Read v Vritable, "	ead value i alue is "0" 0" is read)	s the sam , writing h	e as write as no effe	e value) ect on ope	ration)		

# 11.3.1 Watchdog Timer Control Register (WDTC)

The watchdog timer control register (WDTC) activates or clears the watchdog timer.

#### ■ Watchdog Timer Control Register (WDTC)

000CH CS1	CS0	- R0/\/	- VX R0/		TE3   W	<u>(TE2  WTE1 </u>	WTE0	00000000B
-		100/1						
	└>[v	VTE3	WTE2	WTE1	WTE0	V	/atchdog	control bits
		0		•		<ul> <li>Activate wa (in first wr</li> </ul>	atchdog ti ite after re	mer eset)
		0	1	0	1	<ul> <li>Clear watc (in second)</li> </ul>	hdog time or succe	er eding write after reset)
			Other	than ab	ove	N	o effect o	n operation
	≻	CS1	CS0			Count c	ock switc	h bits
		0	0	Output cycle of time			mebase t	timer (2 <sup>21</sup> /Fсн)
		0	1		Ou	tput cycle of ti	mebase t	timer (2 <sup>20</sup> /Fсн)
		1	0		Ou	tput cycle of w	atch pres	scaler (214/FcL)
		1	1		Ou	tput cycle of w	atch pres	scaler (213/FcL)
R/W : Reada R0,W : Write R0/WX : Undef - : Not us . Initial	able/writabl only (Writa ined bit (Re sed value	e (Rea ble, "C ead va	ad value )" is read alue is "(	e is the s d) D", writir	same as ng has n	write value) o effect on ope	eration)	

#### Figure 11.3-2 Watchdog Timer Control Register (WDTC)

Bit name		Function						
		These bits select the count clock of the watchdog timer.						
		CS1	CS0	Count clock switch bits				
		0	0	Output cycle of timebase timer $(2^{21}/F_{CH})$				
		0	1	Output cycle of timebase timer $(2^{20}/F_{CH})$				
bit7	CS1, CS0:	1	0	Output cycle of watch prescaler $(2^{14}/F_{CL})$				
bit6	Count clock switch bits	1	1	Output cycle of watch prescaler $(2^{13}/F_{CL})$				
		<ul> <li>Write to these control bits.</li> <li>No change ca Note: Always mode, a watch p</li> </ul>	e bits at the sam n be made once select the output is the timebase ti prescaler in single	the time as activating the watchdog timer by the watchdog timer is activated. The watch grescaler in the sub clock mode or sub P mer is stopped in these modes. Do not select the output e system clock product.	atchdog LL clock t of the			
bit5 bit4	Unused bits	These bits are not used. • The read value is "00 <sub>B</sub> ". • Write has no effect on operation						
bit3 to bit0	WTE3, WTE2, WTE1, WTE0: Watchdog control bits	<ul> <li>These bits are used to control the watchdog timer.</li> <li>Writing "0101<sub>B</sub>": activates the watchdog timer (in first write after reset) or clears it (in second or succeeding write after reset).</li> <li>Writing other than "0101<sub>B</sub>": has no effect on operation.</li> <li>The read value is "0000<sub>B</sub>".</li> </ul>						

Table 11.3-1 Functional Description of Each Bit of Watchdog Timer Control Register (WDTC)

Read-modify-write instructions cannot be used.

# 11.4 Explanation of Watchdog Timer Operations and Setup Procedure Example

# The watchdog timer generates a watchdog reset when the watchdog timer counter overflows.

#### Operations of Watchdog Timer

- How to activate the watchdog timer
  - The timer of the watchdog timer is activated when " $0101_B$ " is written to the watchdog control bits of the watchdog timer control register (WDTC:WTE3 to WTE0) for the first time after a reset. The count clock switch bits of the watchdog timer control register (WDTC:CS1,CS0) should also be set at the same time.
  - Once the watchdog timer is activated, a reset is the only way to stop its operation.
- Clearing the watchdog timer
  - When the counter of the watchdog timer is not cleared within the interval time, it overflows, allowing the watchdog timer to generate a watchdog reset.
  - The counter of the watchdog timer is cleared when "0101<sub>B</sub>" is written to the watchdog control bits of the watchdog timer control register (WDTC:WTE3 to WTE0) for the second or any succeeding time.
  - The watchdog timer is cleared at the same time as the timer selected as the count clock (timebase timer or watch prescaler) is cleared.
- Operation in standby mode

Regardless of the clock mode selected, the watchdog timer clears its counter and stops the operation when entering a standby mode (sleep/stop/timebase timer/watch).

Once released from the standby mode, the timer restarts the operation.

Note:

The watchdog timer is also cleared when the timer selected as the count clock (timebase timer or watch prescaler) is cleared.

For this reason, the watchdog timer cannot function as such, if the software is set to clear the selected timer repeatedly during the interval time of the watchdog timer.

#### Interval time

The interval time varies depending on the timing for clearing the watchdog timer. Figure 11.4-1 shows the correlation between the clearing timing of the watchdog timer and the interval time when the timebase timer output  $2^{21}F_{CH}$  (F<sub>CH</sub>: main clock) is selected as the count clock (main clock = 4MHz).





#### • Operation in the sub clock mode

When a watchdog reset is generated in the sub clock mode, the timer starts operating in the main clock mode after the oscillation stabilization wait time has elapsed. The reset signal is outputted during this oscillation stabilization wait time.

#### ■ Setup Procedure Example

The watchdog timer is set up in the following procedure:

1) Select the count clock.	(WDTC:CS1, CS0)
2) Activate the watchdog timer.	(WDTC:WTE3 to WTE0 = $0101_B$ )
3) Clear the watchdog timer.	(WDTC:WTE3 to WTE0 = $0101_B$ )

# 11.5 Precautions when Using Watchdog Timer

#### Care must be taken for the following points when using the watchdog timer.

#### Precautions when Using Watchdog Timer

Stopping the watchdog timer

Once activated, the watchdog timer cannot be stopped until a reset is generated.

#### • Selecting the count clock

The count clock switch bits (WDTC:CS1,0) can be rewritten only when the watchdog control bits (WDTC:WTE3 to WTE0) are set to " $0101_B$ " upon the activation of the watchdog timer. The count clock switch bits cannot be written by a bit operation instruction. Moreover, the bit settings should not be changed once the timer is activated.

In the sub clock mode, the timebase timer does not operate because the main clock stops oscillating.

In order to operate the watchdog timer in the sub clock mode, it is necessary to select the watch prescaler as the count clock beforehand and set "WDTC:CS1,0" to " $10_B$ " or " $11_B$ ".

#### • Clearing the watchdog timer

Clearing the counter used for the count clock of the watchdog timer (timebase timer or watch prescaler) also clears the counter of the watchdog timer.

The counter of the watchdog timer is cleared when entering the sleep mode, stop mode or watch mode.

#### Programming precaution

When creating a program in which the watchdog timer is cleared repeatedly in the main loop, set the processing time of the main loop including the interrupt processing time to the minimum watchdog timer interval time or shorter.

# CHAPTER 12 WATCH PRESCALER

This chapter describes the functions and operations of the watch prescaler.

- 12.1 Overview of Watch Prescaler
- 12.2 Configuration of Watch Prescaler
- 12.3 Registers of the Watch Prescaler
- 12.4 Interrupts of Watch Prescaler
- 12.5 Explanation of Watch Prescaler Operations and Setup Procedure Example
- 12.6 Precautions when Using Watch Prescaler
- 12.7 Sample Programs for Watch Prescaler

### **12.1** Overview of Watch Prescaler

The watch prescaler is a 15-bit down-counting, free-run counter, which is synchronized with the sub clock divided by two. It has an interval timer function that continuously generates interrupt requests at regular intervals.

#### Interval Timer Function

The interval timer function continuously generates interrupt requests at regular intervals, using the sub clock divided by two as its count clock.

- The counter of the watch prescaler counts down and an interrupt request is generated every time the selected interval time has elapsed.
- The interval time can be selected from the following four types:

Table 12.1-1 shows the interval times of the watch prescaler.

#### Table 12.1-1 Interval Times of Watch Prescaler

Internal count clock cycle	Interval time
2/F <sub>CL</sub> (61.0 μs)	$2^{11} \times 2/F_{CL}$ (125ms)
	$2^{12} \times 2/F_{CL}$ (250ms)
	$2^{13} \times 2/F_{CL}$ (500ms)
	$2^{14} \times 2/F_{CL}$ (1.00s)

#### F<sub>CL</sub>: Sub clock

The values in parentheses represent the values achieved when the sub clock operates at 32.768kHz.

Note:

The watch prescaler cannot be used in single system clock product.

# 12.2 Configuration of Watch Prescaler

The watch prescaler consists of the following blocks:

- Watch prescaler counter
- Counter clear circuit
- Interval timer selector
- Watch prescaler control register (WPCR)

#### Block Diagram of Watch Prescaler



#### Figure 12.2-1 Block Diagram of Watch Prescaler

#### • Watch prescaler counter (counter)

This is a 15-bit down-counter that uses the sub clock divided by two as its count clock.

#### • Counter clear circuit

This circuit controls the clearing of the watch prescaler.

#### Interval timer selector

This circuit selects one out of the four bits used for the interval timer among 15 bits available in the watch prescaler counter.

#### Watch prescaler control register (WPCR)

This register selects the interval time, clears the counter, controls interrupts and checks the status.

#### ■ Input Clock

The watch prescaler uses the sub clock divided by two as its input clock (count clock).

#### Output Clock

The watch prescaler supplies its clock to the timer for the oscillation stabilization wait time of the sub clock, the watchdog timer and the watch counter.

# **12.3** Registers of the Watch Prescaler

### Figure 12.3-1 shows the register of the watch prescaler.

## ■ Register of the Watch Prescaler

		Figure	12.3-1	Register	of the W	Vatch Pro	escaler		
Watch Presca	ler Control	Register	(WDTC)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
000B <sub>H</sub>	WTIF	WTIE	-	-	-	WTC1	WTC0	WCLR	00000000 <sub>B</sub>
	R(RM1),W	R/W	R0/WX	R0/WX	R0/WX	R/W	R/W	R0,W	
<ul> <li>R(RM1),W: Readable/writable (Read value is different from write value, "1" is read by read-modify-write (RMW) instruction)</li> <li>R/W: Readable/writable (Read value is the same as write value)</li> <li>R0/WX: Undefined bit (Read value is "0", writing has no effect on operation)</li> <li>R0,W: Write only (Writable, "0" is read)</li> <li> Not used</li> </ul>									

#### 151

# 12.3.1 Watch Prescaler Control Register (WPCR)

The watch prescaler control register (WPCR) is a register used to select the interval time, clear the counter, control interrupts and check the status.

#### ■ Watch Prescaler Control Register (WPCR)



Figure 12.3-2 Watch Prescaler Control Register (WPCR)

Table 12.3-1	Functional	Description of	f Each	<b>Bit of Watch</b>	Prescaler	Control	Register	(WPCR)
--------------	------------	----------------	--------	---------------------	-----------	---------	----------	--------

	Bit name	Function					
bit7	WTIF: Watch interrupt request flag bit	This bit becomes • Interrupt reque "1". Writing "0": se Writing "1": ig • "1" is always r	<ul> <li>This bit becomes "1" when the selected interval time of the watch prescaler has elapsed.</li> <li>Interrupt requests are generated when this bit and the interrupt request enable bit (WTIE) are set to "1".</li> <li>Writing "0": sets this bit to "0".</li> <li>Writing "1": ignored and has no effect on the operation.</li> <li>"1" is always read in read-modify-write (RMW) instruction.</li> </ul>				
bit6	WTIE: Interrupt request enable bit	This bit enables or disables the output of interrupt requests to interrupt controller. <b>Writing ''0'</b> : disables the interrupt request output of the watch prescaler. <b>Writing ''1'</b> : enables the interrupt request output of the watch prescaler. Interrupt requests are outputted when this bit and the watch interrupt request flag bit (WTIF) are set to "1".					
bit5 to bit3	Unused bits	<ul><li>These bits are not used.</li><li>The read value is always "0".</li><li>Write has no effect on the operation.</li></ul>					
		These bits select	the interval time.				
		WTC1	WTC0	Interval time select bits (Sub clock F <sub>CL</sub> = 32.768kHz)			
bit2	WTC1, WTC0:	0	0	$2^{11} \times 2/F_{CL}$ (125ms)			
bit1	interval time select bits	0	1	$2^{12} \times 2/F_{CL}$ (250ms)			
		1	0	$2^{13} \times 2/F_{CL}$ (500ms)			
		1	1	$2^{14} \times 2/F_{CL}$ (1.00s)			
bit0	WCLR: Watch timer initialization bit	<ul> <li>This bit clears the counter for the watch prescaler.</li> <li>Writing "0": ignored and has no effect on the operation.</li> <li>Writing "1": initializes all counter bits to "1".</li> <li>The read value is always "0".</li> <li>Note: When the output of the watch prescaler is selected as the count clock of the watchdog timer, clearing the watch prescaler with this bit also clears the watchdog timer.</li> </ul>			og		

### **12.4** Interrupts of Watch Prescaler

# An interrupt request is generated when the selected interval time of the watch prescaler has elapsed (interval timer function).

#### ■ Interrupts in Operation of Interval Timer Function (Watch Interrupts)

In any mode other than the main stop mode, the watch interrupt request flag bit is set to "1" (WPCR:WTIF = 1), when the watch prescaler counter counts up by using the source oscillation of the sub clock and the time of the interval timer has elapsed. If the interrupt request enable bit is also enabled (WPCR:WTIE = 1) and watch counter start interrupt request enable bit of the watch counter is disabled (WCSR: ISEL0), an interrupt request (IRQ20) occurs from watch prescaler to an interrupt controller.

- Regardless of the value in the WTIE bit, the WTIF bit is set to "1" when the time set by the watch interrupt interval time select bits has been reached.
- When the WTIF bit is set to "1", changing the WTIE bit from the disable state to the enable state (WPCR:WTIE =  $0 \rightarrow 1$ ) immediately generates an interrupt request.
- The WTIF bit cannot be set when the counter is cleared (WPCR:WCLR = 1) at the same time as the selected bit overflows.
- Write "0" to the WTIF bit in the interrupt processing routine to clear an interrupt request to "0".

#### Note:

When enabling the output of interrupt requests (WPCR:WTIE = 1) after canceling a reset, always clear the WTIF bit at the same time (WPCR:WTIF = 0).

#### ■ Interrupts of Watch Prescaler

#### Table 12.4-1 Interrupts of Watch Prescaler

Item	Description
Interrupt condition	Interval time set by "WPCR:WTC1" and "WTC0" has elapsed.
Interrupt flag	WPCR:WTIF
Interrupt enable	WPCR:WTIE

#### Register and Vector Table Related to Interrupts of Watch Prescaler

#### Table 12.4-2 Register and Vector Table Related to Interrupts of Watch Prescaler

Interrupt	Interrupt Interrupt		setup register	Vector table address		
source	request No.	Register	Setting bit	Upper	Lower	
Watch prescaler <sup>*</sup>	IRQ20	ILR5	L20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	

\*: The watch prescaler shares the same interrupt request number and vector table as the watch counter.

Refer to "CHAPTER 8 INTERRUPTS" for the interrupt request numbers and vector tables of all peripheral functions.

#### Note:

If the interval time set for the watch prescaler is shorter than the oscillation stabilization wait time of the sub clock, an interrupt request of the watch prescaler is generated during the oscillation stabilization wait time of the sub clock required for recovery by an external interrupt upon the transition from the sub clock mode or the sub PLL clock mode to the stop mode. To prevent this, set the interrupt request enable bit (WPCR:WTIE) in the watch prescaler control register to "0" to disable interrupts of the watch prescaler when entering the stop mode during the sub clock mode or the sub PLL clock mode.

# 12.5 Explanation of Watch Prescaler Operations and Setup Procedure Example

The watch prescaler operates as an interval timer.

#### Operations of Interval Timer Function (Watch Prescaler)

The counter of the watch prescaler continues to count down using the sub clock divided by two as its count clock as long as the sub clock oscillates.

When cleared (WPCR:WCLR = 1), the counter starts to count down from "7FFF<sub>H</sub>". Once " $0000_{\text{H}}$ " is reached, the counter returns to "7FFF<sub>H</sub>" to continue the count. When the time set by the interrupt interval time select bits is reached during down-counting, the watch interrupt request flag bit (WPCR:WTIF) is set to "1" in any mode other than the main stop mode. In other words, a watch interrupt request is generated at each selected interval time, based on the time when the counter was last cleared.

#### Clearing Watch Prescaler

If the watch prescaler is cleared when the output of the watch prescaler is used in other peripheral functions, this will affect the operation by changing the count time or in other manners.

When clearing the counter by using the watch prescaler initialization bit (WTCR:WCLR), perform setup so that this does not have unexpected effects on other peripheral functions.

When the output of the watch prescaler is selected as the count clock, clearing the watch prescaler also clears the watchdog timer.

The watch prescaler is cleared not only by the watch prescaler initialization bit (WTCR:WCLR) but also when the sub clock is stopped and a count is required for the oscillation stabilization wait time.

- When moving from the sub clock mode or sub PLL clock mode to the stop mode
- When the sub clock oscillation stop bit in the system clock control register (SYCC:SUBS) is set to "1" in the main clock mode or main PLL clock mode

In addition, the counter of the watch prescaler is cleared and stops operation when a reset is generated.

#### Operating Examples of Watch Prescaler

Figure 12.5-1 shows operating examples under the following conditions:

- 1) When a power-on reset is generated
- 2) When entering the sleep mode during the operation of the interval timer function in the sub clock mode or sub PLL clock mode
- 3) When entering the stop mode during the operation of the interval timer function in the sub clock mode or sub PLL clock mode
- 4) When a request is issued to clear the counter

The same operation is performed when changing to the watch mode as for when changing to the sleep mode.



Figure 12.5-1 Operating Examples of Watch Prescaler

#### The watch prescaler is set up in the following procedure:

#### Initial setup

1) Set the interrupt level.	(ILR5)
2) Set the interval time.	(WPCR:WTC1, WTC0)
3) Enable interrupts.	(WPCR:WTIE = 1)
4) Clear the counter.	(WPCR:WCLR = 1)

#### Processing interrupts

- 1) Clear the interrupt request flag. (WPCR:WTIF = 0)
- 2) Process any interrupt.

# 12.6 Precautions when Using Watch Prescaler

# Shown below are the precautions that must be followed when using the watch prescaler.

The watch prescaler cannot be used in single system clock option product.

#### Precautions when Using Watch Prescaler

• When setting the prescaler by program

The prescaler cannot be recovered from interrupt processing when the watch interrupt request flag bit (WPCR:WTIF) is set to "1" and the interrupt request enable bit is enabled (WPCR:WTIE = 1). Always clear the WTIF bit within the interrupt routine.

#### • Clearing the watch prescaler

When the watch prescaler is selected as the count clock of the watchdog timer (WDTC:CS1, CS0 =  $10_B$  or CS1, CS0 =  $11_B$ ), clearing the watch prescaler also clears the watchdog timer.

#### • Watch interrupts

In the main stop mode, the watch prescaler performs counting but does not generate the watch prescaler interrupts (IRQ20).

#### Peripheral functions receiving clock from the watch prescaler

If the watch prescaler is cleared when the output of the watch prescaler is used in other peripheral functions, this will affect the operation by changing the count time or in other manners.

The clock for the watchdog timer is also outputted from the initial state. However, as the watchdog timer counter is cleared at the same time as the prescaler counter, the watchdog timer operates in the normal cycles.

# 12.7 Sample Programs for Watch Prescaler

#### We provide sample programs that can be used to operate the watch prescaler.

#### Sample Programs for Watch Prescaler

For information about sample programs for the watch prescaler, refer to "Sample programs" in Preface.

#### Setup Methods without Sample Program

How to initialize the watch prescaler

The watch timer initialization bit (WPCR:WCLR) is used.

What to be controlled	Watch timer initialization bit (WCLR)
When initializing watch prescaler	Set the bit to "1"

#### How to select the interval time

The watch interrupt interval time select bits (WPCR:WTC1/WTC0) are used to select the interval time.

#### Interrupt-related register

The interrupt level register shown in the following table is used to select the interrupt level.

Interrupt source	Interrupt level setup register	Interrupt vector
Watch prescaler	Interrupt level register (ILR5) Address: 0007E <sub>H</sub>	#20 Address: 0FFD2 <sub>H</sub>

#### • How to enable/disable/clear interrupts

Interrupt request enable flag, Interrupt request flag

The interrupt request enable bit (WPCR:WTIE) is used to enable interrupts.

What to be controlled	Interrupt request enable bit (WTIE)
When disabling interrupt requests	Set the bit to "0"
When enabling interrupt requests	Set the bit to "1"

The watch interrupt request flag (WPCR:WTIF) is used to clear interrupt requests.

What to be controlled	Watch interrupt request flag (WTIF)
When clearing interrupt requests	Write "0"

#### CHAPTER 12 WATCH PRESCALER

# CHAPTER 13 WATCH COUNTER

This chapter describes the functions and operations of the watch counter.

- 13.1 Overview of Watch Counter
- 13.2 Configuration of Watch Counter
- 13.3 Registers of Watch Counter
- 13.4 Interrupts of Watch Counter
- 13.5 Explanation of Watch Counter Operations and Setup Procedure Example
- 13.6 Precautions when Using Watch Counter
- 13.7 Sample Programs for Watch Counter

### 13.1 Overview of Watch Counter

# The watch counter can generate interrupt requests ranging from min. 125ms to max. 63s intervals.

#### Watch Counter

The watch counter performs counting for the number of times specified in the register by using the selected count clock and generates an interrupt request. The count clock can be selected from the four types shown in Table 13.1-1. The count value can be set to any number from 0 to 63. When "0" is selected, no interrupt is generated.

When the count clock is set to 1s and the count value is set to "60", an interrupt is generated every one minute.

Count clock	Count cycle when F <sub>CL</sub> operates at 32.768kHz
$2^{12}/F_{CL}$	125ms
$2^{13}/F_{CL}$	250ms
$2^{14}/F_{CL}$	500ms
$2^{15}/F_{CL}$	1s

F<sub>CL</sub>: Sub clock

# **13.2** Configuration of Watch Counter

#### Figure 13.2-1 shows the block diagram of the watch counter.

#### Block Diagram of Watch Counter



• Counter

This is a 6-bit down-counter that uses the output clock of the watch prescaler as its count clock.

#### • Watch counter control register (WCSR)

This register controls interrupts and checks the status.

• Watch counter data register (WCDR)

This register sets the interval time and selects the count clock.

#### ■ Input Clock

The watch counter uses the output clock of the watch prescaler as its input clock (count clock).
#### 13.3 **Registers of Watch Counter**

## Figure 13.3-1 shows the registers of the watch counter.

## ■ Registers of Watch Counter

Address	bit7	, ,	hit5	hit/	hit3	hit?	hit1	hitO	Initial value
					DILJ				
UFE3H	CS1	CSO	RCTR5	RCTR4	RCTR3	RCTR2	RCTR1	RCIRO	OUTTITIE
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
valori counter c	/onlight logi								
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address 0070 <sub>H</sub>	bit7	bit6 WCFLG	bit5 CTR5	bit4 CTR4	bit3 CTR3	bit2 CTR2	bit1 CTR1	bit0 CTR0	Initial value 00000000 <sub>E</sub>

## 13.3.1 Watch Counter Data Register (WCDR)

The watch counter data register (WCDR) is used to select the count clock and set the counter reload value.

## ■ Watch Counter Data Register (WCDR)



## Figure 13.3.1-1 Watch Counter Data Register (WCDR)

## Table 13.3.1-1 Functional Description of Each Bit of Watch Counter Data Register (WCDR)

	Bit name	Function
bit7 bit6	CS1, CS0: Count clock select bits	These bits select the clock for the watch counter. $00_B = 2^{12}/F_{CL}, 01_B = 2^{13}/F_{CL}, 10_B = 2^{14}/F_{CL}, 11_B = 2^{15}/F_{CL}$ (F <sub>CL</sub> : Sub clock) These bits should be modified when the WCSR:ISEL bit is "0".
bit5 bit4 bit3 bit2 bit1 bit0	RCTR5 to RCTR0: Counter reload value setting bits	These bits set the counter reload value. If the value is modified during counting, the modified value will become effective upon a reload after the counter underflows. <b>Writing ''0''</b> : generates no interrupt request. If the reload value (RCTR5 to RCTR0) is modified at the same time as an interrupt is generated (WCSR:WCFLG = 1), the correct value will not be reloaded. Therefore, the reload value must be modified before an interrupt is generated, such as when the watch counter is stopped (WCSR:ISEL bit = 0), during the interrupt routine.

## 13.3.2 Watch Counter Control Register (WCSR)

The watch counter control register (WCSR) is used to control the operation and interrupts of the watch counter. It can also read the count value.

## ■ Watch Counter Control Register (WCSR)



#### Figure 13.3.2-1 Watch Counter Control Register (WCSR)

	Bit name	Function
bit7	ISEL: Watch counter start & interrupt request enable bit	<ul> <li>This bit activates the watch counter and selects whether to enable interrupts of the watch counter or those of the watch prescaler.</li> <li>When set to "0":The watch counter is cleared and stopped. Moreover, interrupt requests of the watch counter are disabled, while interrupt requests of the watch prescaler are enabled.</li> <li>When set to "1":The interrupt request output of the watch counter is enabled and the counter starts operation. On the other hand, interrupt requests of the watch prescaler are disabled.</li> <li>Always disable interrupts of the watch prescaler before setting this bit to "1" to select interrupts of the watch counter.</li> <li>The watch counter performs counting, using an asynchronous clock from the watch prescaler. For this reason, an error of up to one count clock may occur at the beginning of a count cycle, depending on the timing for setting ISEL bit to "1".</li> </ul>
bit6	WCFLG: Interrupt request flag bit	<ul> <li>This bit is set to "1" when the counter underflows.</li> <li>When this bit and the ISEL bit are both set to "1", a watch counter interrupt is generated.</li> <li>Writing "0" clears the bit.</li> <li>Writing "1" has no effect on the operation.</li> <li>"1" is always read in read-modify-write (RMW) instruction.</li> </ul>
bit5 bit4 bit3 bit2 bit1 bit0	CTR5 to CTR0: Counter read bits	<ul> <li>These bits can read the counter value during counting. It should be noted that the correct counter value may not be read if a read is attempted while the counter value is being changed. Therefore, read the counter value twice to check if the same value is read on both occasions before using it.</li> <li>Write has no effect on the operation.</li> </ul>

## Table 13.3.2-1 Functional Description of Each Bit of Watch Counter Status Register (WCSR)

## 13.4 Interrupts of Watch Counter

# The watch counter outputs interrupt requests when the counter underflows (counter value = $000001_{B}$ ).

## Interrupts of Watch Counter

When the counter of the watch counter underflows, the interrupt request flag bit (WCFLG) of the watch counter control register (WCSR) is set to "1". If the interrupt request enable bit (ISEL) of the watch counter is set to "1", an interrupt request of the watch counter is outputted to the interrupt controller.

Table 13.4-1 shows the interrupt control bits and interrupt sources of the watch counter.

#### Table 13.4-1 Interrupt Control Bits and Interrupt Sources of Watch Timer

Item	Description
Interrupt request flag bit	WCFLG bit of the WCSR register
Interrupt request enable bit	ISEL bit of the WCSR register
Interrupt source	Counter underflow

## Register and Vector Table Related to Interrupts of Watch Counter

Interrupt	Interrupt Interrupt source request No.	Interrupt level	setup register	Vector table address		
source		Register	Setting bit	Upper	Lower	
Watch counter*	IRQ20	ILR5	L20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	

Refer to "CHAPTER 8 INTERRUPTS" for the interrupt request numbers and vector tables of all peripheral functions.

\*: The watch counter shares the same interrupt request number and vector table as the watch prescaler.

## 13.5 Explanation of Watch Counter Operations and Setup Procedure Example

The watch counter counts down for the number of times specified in the count value by RCTR5 to RCTR0 bits, using the count clock selected by CS1 and CS0 bits, when the ISEL bit is set to "1". Once the counter underflows, WCFLG bit of the WCSR register is set to "1", generating an interrupt.

## Setup Procedure of Watch Counter

The setup procedure of the watch counter is described below.

- (1) Select the count clock (CS1 and CS0 bits) and set the counter reload value (RCTR5 to RCTR0 bits).
- (2) Set the ISEL bit of the WCSR register to "1" to start a down count and enable interrupts. Also disable interrupts of the watch prescaler.

The watch counter performs counting by using a divided clock (asynchronous) from the watch prescaler. An error of up to one count clock may occur at the beginning of a count cycle, depending on the timing for setting the ISEL bit to "1".

- (3) When the counter underflows, the WCFLG bit of the WCSR register is set to "1", generating an interrupt.
- (4) Write "0" to the WCFLG bit to clear it.
- (5) If RCTR5 to RCTR0 bits are modified during counting, the reload value will be updated during a reload after the counter is set to "1".
- (6) When writing "0" to the ISEL bit, the counter becomes "0" and stops operation.



#### Figure 13.5-1 Descriptive Diagram of Watch Counter Operation

Note:

When the operation is reactivated by WCSR:ISEL=0 after counter stop, please reactivate after confirming reading WCSR:CTR[5:0] twice, and clearing to  $CTR[5:0]=000000_B$ .

## Operation in Sub Stop Mode

When the device enters the sub stop mode, the watch counter stops the count operation and the watch prescaler is also cleared. Therefore, the watch counter cannot count the correct value after the sub stop mode is cancelled, the ISEL bit must always be set to "0" to clear the counter before use. In any standby mode other than the sub stop mode, the watch counter continues to operate.

## Operation at the Main Stop Mode

The interrupt is not generated though the clock counter continues the count operation when entering the main stop mode. Moreover, the clock counter stops, too, when sub clock oscillation stop bit (SYCC: SUBS) of the system clock control register is set to "1".

## Setup Procedure Example

The watch counter is set up in the following procedure:

### Initial setup

1) Set the interrupt level.	(ILR5)
2) Select the count clock.	(WCDR:CS1, CS0)
3) Set the counter reload value.	(WCDR:RCTR5 to RCTR0)
4) Activate the watch counter and enable interrupts.	(WCDR:ISEL = 1)

#### Interrupt processing

1) Clear the interrupt request flag. (WCSR:WCFLG = 0)

2) Process any interrupt.

## 13.6 Precautions when Using Watch Counter

## Shown below are the precautions that must be followed when using the watch counter.

- If the watch prescaler is cleared during the operation of the watch counter, the watch counter may not be able to perform normal operation. When clearing the watch prescaler, set the ISEL bit of the WCSR register to "0" to stop the watch counter in advance.
- When the operation is reactivated by WCSR:ISEL=0 after counter stop, please reactivate after confirming reading WCSR:CTR[5:0] twice, and clearing to CTR[5:0]=000000<sub>B</sub>.

## 13.7 Sample Programs for Watch Counter

## We provide sample programs that can be used to operate the watch counter.

## Sample Programs for Watch Counter

For information about sample programs for the watch counter, refer to " Sample Programs" in Preface.

## Setup Methods without Programs

• How to enable/stop the watch counter

Use the interrupt request enable bit (WCSR:ISEL).

What to be controlled	Watch timer initialization bit (ISEL)
When enabling watch counter	Set the bit to "1"
When stopping watch counter	Set the bit to "0"

### • How to select the count clock

The count clock select bits (WCDR:CS1/CS0) are used to select the clock.

### Interrupt-related register

The interrupt level is set in the interrupt level register shown in the following table.

Interrupt source	Interrupt level setup register	Interrupt vector
Watch counter	Interrupt level register (ILR5) Address: 0007E <sub>H</sub>	#20 Address: 0FFD2 <sub>H</sub>

#### How to enable/disable/clear interrupts

Interrupt request enable flag, Interrupt request flag

The interrupt request enable bit (WCSR:ISEL) is used to enable interrupts.

What to be controlled	Interrupt request enable bit (ISEL)
When disabling interrupt request	Set the bit to "0"
When enabling interrupt request	Set the bit to "1"

The interrupt request flag (WCSR:WCFLG) is used to clear interrupt requests.

What to be controlled	Interrupt request flag (WCFLG)
When clearing interrupt request	Write "0"

## CHAPTER 13 WATCH COUNTER

# CHAPTER 14 WILD REGISTER

This chapter describes the functions and operations of the wild register.

- 14.1 Overview of Wild Register
- 14.2 Configuration of Wild Register
- 14.3 Registers of Wild Register
- 14.4 Operating Description of Wild Register
- 14.5 Typical Hardware Connection Example

## 14.1 Overview of Wild Register

The wild register can be used to patch bugs in the program by using the addresses set in the built-in register and amendment data.

The following section describes the wild register function.

## Wild Register Function

The wild register consists of 3 data setup registers, 3 upper-address setup registers, 3 lower-address setup registers, a 1-byte address compare enable register and a 1-byte data test setup register. When certain addresses and modified data are specified in these registers, the ROM data can be replaced with the modified data specified in the registers. Data of up to three different addresses can be modified.

The wild register function can be used to debug the program after creating the mask and patch bugs in the program.

## 14.2 Configuration of Wild Register

The block diagram of the wild register is shown below. The wild register consists of the following blocks:

- Memory area block
   Wild register data setup register (WRDR0 to WRDR2)
   Wild register address setup register (WRAR0 to WRAR2)
   Wild register address compare enable register (WREN)
   Wild register data test setup register (WROR)
- Control circuit block

## Block Diagram of Wild Register Function



## Figure 14.2-1 Block Diagram of Wild Register Function

#### Memory area block

The memory area block consists of the wild register data setup registers (WRDR), wild register address setup registers (WRAR), wild register address compare enable register (WREN) and wild register data test setup register (WROR). The wild register function is used to specify the addresses and data that need to be replaced. The wild register address compare enable register (WREN) enables the wild register function for each wild register data setup register (WROR). Moreover, the wild register data test setup register (WROR) enables the normal read function for each wild register data setup register (WRDR).

#### • Control circuit block

This circuit compares the actual address data with addresses set in the wild register address setup registers (WRDR), and if the values match, outputs the data from the wild register data setup register (WRDR) to the data bus. The control circuit block uses the wild register address compare enable register (WREN) to control the operation.

## 14.3 Registers of Wild Register

The registers of the wild register include the wild register data setup registers (WRDR), wild register address setup registers (WRAR), wild register address compare enable register (WREN) and wild register data test setup register (WROR).

## Registers Related to Wild Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F82 <sub>H</sub> WRDR0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
0F85 <sub>H</sub> WRDR1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	2
0F88 <sub>H</sub> WRDR2									
Wild register address setup r	egisters (	WRAR	) to WRA	AR2)					
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0F80 <sub>H</sub> , 0F81 <sub>H</sub> WRAR0	RA15							RA8	00000000 <sub>B</sub>
0F83 <sub>H</sub> , 0F84 <sub>H</sub> WRAR1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	1
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F86 <sub>H</sub> , 0F87 <sub>H</sub> WRAR2	RA7							RA0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	2
Wild register address compared	re enable	registe	r (WREN	I)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0076 <sub>H</sub> WREN	-	-	Reserved	Reserved	Reserved	EN2	EN1	EN0	00000000 <sub>B</sub>
	R0/WX	R0/WX	R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	
Wild register data test setup	register (	WROR)							
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address		_	Reserved	Reserved	Reserved	DRR2	DRR1	DRR0	00000000 <sub>B</sub>
Address 0077 <sub>H</sub> WROR	-	-			DOANO	D 444	5 4 4 4	D 44/	1
Address 0077 <sub>H</sub> WROR	- R0/WX	R0/WX	R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	

Figure 14.3-1 Registers Related to Wild Register

## ■ Wild Register Number

Each wild register address setup register (WRAR) and wild register data setup register (WRDR) has its corresponding wild register number.

## Table 14.3-1 Wild Register Numbers Corresponding to Wild Register Address Setup Registers and Wild Register Data Setup Registers

Wild register number	Wild register address setup register (WRAR)	Wild register data setup register (WRDR)
0	WRAR0	WRDR0
1	WRAR1	WRDR1
2	WRAR2	WRDR2

## 14.3.1 Wild Register Data Setup Registers (WRDR0 to WRDR2)

The wild register data setup registers (WRDR0 to WRDR2) use the wild register function to specify the data to be amended.

## ■ Wild Register Data Setup Registers (WRDR0 to WRDR2)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F82 <sub>H</sub>	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
	R/W								
WRDR1									
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F85 <sub>H</sub>	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
	R/W								
VRDR2									
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F88 <sub>H</sub>	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
	R/W								

## Figure 14.3-2 Wild Register Data Setup Registers (WRDR0 to WRDR2)

## Table 14.3-2 Functional Description of Each Bit of Wild Register Data Setup Resister (WRDR)

I	Bit name	Function
bit7 F to V bit0 s	RD7 to RD0: Wild register data setup bits	<ul> <li>These bits specify the data to be amended by the wild register function.</li> <li>These bits are used to set the amendment data at the address assigned by the wild register address setup register (WRAR). Data is enabled at the address corresponding to each wild register number.</li> <li>Read access of these bits is enabled only when the corresponding data test setting bit in the wild register data test setup register (WROR) is set to "1".</li> </ul>

# 14.3.2 Wild Register Address Setup Registers (WRAR0 to WRAR2)

The wild register address setup registers (WRAR0 to WRAR2) set the address to be amended by the wild register function.

## Wild Register Address Setup Registers (WRAR0 to WRAR2)

WRAR0									
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0F80 <sub>H</sub>	RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F81 <sub>H</sub>	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WRART									
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0F83 <sub>H</sub>	RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Adross	hit7	hite	hit5	hit/	hit?	hita	hit1	hitO	Initial value
Address		DILO			DIG				
0F04 <sub>H</sub>					RAJ		RAI		0000000B
	R/11	R/VV	R/ VV	K/ VV	K/ VV	K/ VV	R/ V V	K/ VV	
WRAR2									
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0F86 <sub>H</sub>	RA15	RA14	RA13	RA12	RA11	RA10	RA9	RA8	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0F87 <sub>H</sub>	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
R/W: Readable/wi	itable (R	ead valu	e is the	same as	write va	lue)			

## Figure 14.3-3 Wild Register Address Setup Registers (WRAR0 to WRAR2)

## Table 14.3-3 Functional Description of Each Bit of Wild Register Address Setup Register (WRAR)

	Bit name	Function
bit15	RA15 to RA0:	These bits set the address to be amended by the wild register function.
to bit0	Wild register address setting bits	These bits are used to specify the address to be allocated. The address is specified in accordance with its corresponding wild register number.

## 14.3.3 Wild Register Address Compare Enable Register (WREN)

The wild register address compare enable register (WREN) enables/disables the operation of the wild register in accordance with each wild register number.

## ■ Wild Register Address Compare Enable Register (WREN)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0076 <sub>H</sub>	-	-	Reserved	Reserved	Reserved	EN2	EN1	EN0	00000000 <sub>B</sub>
	R0/WX	R0/WX	R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	
R0/WA : Undefined bit (Read value is "0", writing has no effect on operation) R0/W0 : Reserved bit (Write value is "0", read value is "0") R/W : Readable/writable (Read value is the same as write value)									

## Table 14.3-4 Functional Description of Wild Register Address Compare Enable Register (WREN)

	Bit name	Function
bit7 bit6	Unused bits	<ul><li>These bits are not used.</li><li>The read value is "0".</li><li>Write has no effect on the operation.</li></ul>
bit5 to bit3	Reserved bits	These bits are reserved. <ul> <li>The read value is "0".</li> <li>Always set "0".</li> </ul>
bit2 to bit0	EN2, EN1, EN0: Wild register address compare enable bits	<ul> <li>These bits enable/disable the operation of the wild register.</li> <li>EN0 corresponds to wild register number 0.</li> <li>EN1 corresponds to wild register number 1.</li> <li>EN2 corresponds to wild register number 2.</li> <li>When set to "0": disable the operation of the wild register function.</li> <li>When set to "1": enable the operation of the wild register function.</li> </ul>

## 14.3.4 Wild Register Data Test Setup Register (WROR)

The wild register data test setup register (WROR) enables/disables reading from the corresponding wild register data setup register (WRDR0 to WRDR2).

## ■ Wild Register Data Test Setup Register (WROR)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0077 <sub>H</sub>	-	-	Reserved	Reserved	Reserved	DRR2	DRR1	DRR0	00000000 <sub>B</sub>
	R0/WX	R0/WX	R0/W0	R0/W0	R0/W0	R/W	R/W	R/W	
R0/WX : Undefined bit (Read value is "0", writing has no effect on operation) R0/W0 : Reserved bit (Write value is "0", read value is "0") R/W : Readable/writable (Read value is the same as write value) -: Not used									

## Table 14.3-5 Functional Description of Wild Register Data Test Setup Register (WROR)

	Bit name	Function
bit7 bit6	Unused bits	<ul><li>These bits are not used.</li><li>The read value is "0".</li><li>Write has no effect on operation.</li></ul>
bit5 to bit3	Reserved bits	These bits are reserved. <ul> <li>The read value is "0".</li> <li>Always set "0".</li> </ul>
bit2 to bit0	DRR2, DRR1, DRR0: Wild register data test setting bits	<ul> <li>These bits enable/disable the normal reading from the corresponding data setup register of the wild register.</li> <li>DRR0 enables/disables reading from the wild register data setup register (WRDR0).</li> <li>DRR1 enables/disables reading from the wild register data setup register (WRDR1).</li> <li>DRR2 enables/disables reading from the wild register data setup register (WRDR2).</li> <li>When set to "0": disable reading.</li> <li>When set to "1": enable reading.</li> </ul>

## 14.4 Operating Description of Wild Register

## This section describes the setup procedure for the wild register.

## Setup Procedure for Wild Register

Prepare a special program that can read the value to be set in the wild register from external memory (e.g.  $E^2$ PROM or FRAM) in the user program before executing the program. The setup method for the wild register is shown below.

It should be noted that this section does not explain how to communicate between the external memory and the device.

- Write the address of the built-in ROM code that will be modified to the wild register address setup register (WRAR0 to WRAR2).
- Write a new code into the corresponding wild register data setup register (WRDR0 to WRDR2).
- Write to the corresponding bits in the wild register address compare enable register (WREN) to enable the wild register function.

Table 14.4-1 shows the register setup procedure for the wild register.

Table 14.4-1 Register Setup Procedure for Wild Register

Operating step	Operation	Example operation
1	Read replacement data from outside through its specific communication method.	Set the built-in ROM code to be modified is in the address $F011_{H}$ and the data to be modified to " $B5_{H}$ ". Three built-in ROM codes can be modified.
2	Write the replacement address into the wild register address setup register (WRAR0 to WRAR2).	Set wild register address setup registers (WRAR0 = $F011_{H}$ , WRAR1 =, WRAR2 =).
3	Write a new ROM code (replacement for the built-in ROM code) to the wild register data setup register (WRDR0 to WRDR2).	Set the wild register data setup registers (WRDR0 = $B5_H$ , WRDR1 =, WRDR2 =).
4	Enable the corresponding bits in the wild register address compare enable register (WREN).	Setting bit 0 of the address compare enable register (WREN) to "1" enables the wild register function for the wild register number 1. If the address matches the value set in the address setup register (WRAR), the value of the data setup register (WRDR) will replace the built-in ROM code. When replacing more than one built-in ROM code, enable the corresponding bits of the address compare enable register (WREN).

## Wild Register Applicable Addresses

The wild register is applicable to all addresses in the address space except " $0078_{\text{H}}$ ".

As address " $0078_{\text{H}}$ " is used as a mirror address for the register bank pointer and direct bank pointer, this address cannot be patched.

## 14.5 **Typical Hardware Connection Example**

Shown below is a typical hardware connection example applied when using the wild register function.

## ■ Hardware Connection Example





# CHAPTER 15 8/16-BIT COMPOUND TIMER

This chapter describes the functions and operations of the 8/16-bit compound timer.

- 15.1 Overview of 8/16-bit Compound Timer
- 15.2 Configuration of 8/16-bit Compound Timer
- 15.3 Channels of 8/16-bit Compound Timer
- 15.4 Pins of 8/16-bit Compound Timer
- 15.5 Registers of 8/16-bit Compound Timer
- 15.6 Interrupts of 8/16-bit Compound Timer
- 15.7 Operating Description of Interval Timer Function (One-shot Mode)
- 15.8 Operating Description of Interval Timer Function (Continuous Mode)
- 15.9 Operating Description of Interval Timer Function (Free-run Mode)
- 15.10 Operating Description of PWM Timer Function (Fixed-cycle mode)
- 15.11 Operating Description of PWM Timer Function (Variable-cycle Mode)
- 15.12 Operating Description of PWC Timer Function
- 15.13 Operating Description of Input Capture Function
- 15.14 Operating Description of Noise Filter
- 15.15 States in Each Mode during Operation
- 15.16 Precautions when Using 8/16-bit Compound Timer

## 15.1 Overview of 8/16-bit Compound Timer

The 8/16-bit compound timer consists of two 8-bit counters and can be used as two 8bit timers, or one 16-bit timer if they are connected in cascade.

The 8/16-bit compound timer has the following functions:

- Interval timer function
- PWM timer function
- PWC timer function (pulse width measurement)
- Input capture function

## Interval Timer Function (One-shot Mode)

When the interval timer function (one-shot mode) is selected, the counter starts counting from " $00_{\text{H}}$ " as the timer is started. When the counter value matches the register setting value, the timer output is inverted, the interrupt request occurs, and the count operation is stopped.

## Interval Timer Function (Continuous Mode)

When the interval timer function (continuous mode) is selected, the counter starts counting from " $00_{\text{H}}$ " as the timer is started. When the counter value matches the register setting value, the timer output is inverted, the interrupt request occurs, and the count operation is continued from " $00_{\text{H}}$ " again. The timer output a square wave as a result of this repeated operation.

## Interval Timer Function (Free-run Mode)

When the interval timer function (free-run mode) is selected, the counter starts counting from " $00_{\text{H}}$ ". When the counter value matches the register setting value, the timer output is inverted and the interrupt request occurs. When the counter continues to count until reaching "FF<sub>H</sub>", it restarts counting from " $00_{\text{H}}$ " to continue the counting operation. The timer outputs a square wave as a result of this repeated operation.

## PWM Timer Function (Fixed-cycle Mode)

When the PWM timer function (fixed-cycle mode) is selected, a PWM signal with a variable "H" pulse width is generated in fixed cycles. The cycle is fixed to " $FF_H$ " during 8-bit operation or " $FFFF_H$ " during 16-bit operation. The time is determined by the count clock selected. The "H" pulse width is specified by setting a register.

## PWM Timer Function (Variable-cycle Mode)

When the PWM timer function (variable-cycle mode) is selected, two 8-bit counters are used to generate an 8-bit PWM signal in any cycles and duty depending on the cycle and "L" pulse width specified by registers.

In this operation mode, the compound timer cannot serve as a 16-bit counter, as two 8-bit counters are used.

## PWC Timer Function

When the PWC timer function is selected, the width and cycle of an external input pulse can be measured. In this operation mode, the counter starts counting from " $00_{\text{H}}$ " upon detection of a count start edge of an external input signal and transfers the count value to a register to generate an interrupt upon detection of a count end edge.

## ■ Input Capture Function

When the input capture function is selected, the counter value is stored in a register upon detection of an edge for an external input signal.

This function is available in either free-run mode or clear mode for count operation.

In the clear mode, the counter starts counting from " $00_{\text{H}}$ " and transfers its value to a register to generate an interrupt upon detection of an edge. In this case, the counter continues to count from " $00_{\text{H}}$ ".

In the free-run mode, the counter transfers its value to a register to generate an interrupt upon detection of an edge. In this case, however, the counter continues to count without being cleared.

## 15.2 Configuration of 8/16-bit Compound Timer

The 8/16-bit compound timer consists of the following blocks:

- 8-bit counter × 2 channels
- 8-bit comparator (including a temporary latch) × 2 channels
- 8/16-bit compound timer 00/01 data register × 2 channels (T00DR/T01DR)
- 8/16-bit compound timer 00/01 control status register 0  $\times$  2 channels (T00CR0/ T01CR0)
- 8/16-bit compound timer 00/01 control status register 1  $\times$  2 channels (T00CR1/ T01CR1)
- 8/16-bit compound timer 00/01 timer mode control register (TMCR0)
- Output controller × 2 channels
- Control logic × 2 channels
- Count clock selector × 2 channels
- Edge detector × 2 channels
- Noise filter × 2 channels



## Block Diagram of 8/16-bit Compound Timer



This counter serves as the basis for various timer operations. It can be used either as two 8-bit counters or as a 16-bit counter.

#### • 8-bit comparator

The comparator compares the values in the 8/16-bit compound timer 00/01 data register and counter. It incorporates a latch to temporarily store the 8/16-bit compound timer 00/01 data register value.

## 8/16-bit compound timer 00/01 data register

The 8/16-bit compound timer 00/01 data register is used to write the maximum value counted during interval timer or PWM timer operation and to read the count value during PWC timer or input capture operation.

8/16-bit compound timer 00/01 control status registers 0 (T00CR0/T01CR0)

These registers are used to select the timer operation mode, select the count clock, and to enable or disable IF flag interrupts.

8/16-bit compound timer 00/01 control status registers 1 (T00CR1/T01CR1)

These registers are used to control interrupt flags, timer output, and timer operation.

8/16-bit compound timer 00/01 timer mode control register (TMCR0)

This register is used to select the noise filter function, 8-bit or16-bit operation mode, and signal input to timer 00 and to indicate the timer output value.

#### Output controller

The output controller controls timer output. The timer output is supplied to the external pin when the pin output has been enabled.

#### Control logic

The control logic controls timer operation.

#### Count clock selector

The selector selects the counter operation clock signal from among prescaler outputs (machine clock divided signal and timebase timer output).

#### Edge detector

The edge detector selects the edge of an external input signal to be used as an event for PWC timer operation or input capture operation.

Noise filter

This filter serves as a noise filter for external input signals. "H" pulse noise, "L" pulse noise, or "H"/"L"-pulse noise elimination can be selected as the filter function.

#### TII0 internal pin (internally connected to the LIN-UART, available only in channel 0)

The TII0 pin serves as the signal input pin for timer 00; it is connected to the LIN-UART inside the chip. For information about how to use the pin, refer to "CHAPTER 22 LIN-UART". Note that the TII0 pin in channel 1 is internally fixed to "0".

#### Input Clock

The 8/16-bit compound timer uses the output clock from the prescaler as its input clock (count clock).

## 15.3 Channels of 8/16-bit Compound Timer

## This section describes the channels of 8/16-bit compound timer.

## ■ Channels of 8/16-bit Compound Timer

MB95130/M series contains one channel of 8/16-bit compound timer.

In one channel, there are two 8-bit counters. Each counter can be used as two 8-bit timers or one 16-bit timer. The following table lists the external pins and registers corresponding to each channel.

Table 15.3-1 8/16-bit Compound Timer Channels and Corresponding External Pins

Channel	Pin name	Pin function
	TO00	Timer 00 output
0	TO01	Timer 01 output
	EC0	Timer 00 input and timer 01 input

Channel	Register name	Registers
	T00CR0	Timer 00 control status register 0
	T01CR0	Timer 01 control status register 0
	T00CR1	Timer 00 control status register 1
0	T01CR1	Timer 01 control status register 1
	T00DR	Timer 00 data register
	T01DR	Timer 01 data register
	TMCR0	Timer 00/01 timer mode control register

Table 15.3-2	8/16-bit Com	pound Timer	Channels and	Correspond	lina Reaisters
					ing nogiotoro

The 2-digit number in the pin names and register names corresponds to channel and timer. The upper number corresponds to channel and the lower number corresponds to timer.

## 15.4 Pins of 8/16-bit Compound Timer

## This section describes the pins related to the 8/16-bit compound timer.

## Pins Related to 8/16-bit Compound Timer

The external pins related to the 8/16-bit compound timer are TO00, TO01, and EC0. TII0 is for internal chip connection.

#### TO00 pins

TO00:

This pin serves as the timer output pin for timer 00 during 8-bit operation or for timers 00 and 01 during 16-bit operation. When the output is enabled (T00CR1:OE = 1) in interval timer, PWM timer, or PWC timer function, the pin is set for output automatically regardless of the port direction register (DDR2:bit2) to serve as the timer output TO00 pin.

The output remains indeterminate when the input capture function has been selected enabling output.

#### TO01 pins

TO01:

This pin serves as the timer output pin for timer 01 during 8-bit operation. When the output is enabled (T00CR1:OE = 1) in interval timer, PWM timer (fixed cycle mode), or PWC timer function, the pin is set for output automatically regardless of the port direction register (DDR2:bit3) to serve as the timer output TO01 pin.

The output remains indeterminate during 16-bit operation when the PWM timer function (variable-cycle mode) or input capture function has been selected enabling output.

#### EC0 pins

The EC0 pin is connected to the EC00 and EC01 internal pins.

#### EC00 internal pin:

This pin serves as the external count clock input pin for timer 00 when the interval timer or PWM timer function has been selected, or as the signal input pin for timer 00 when the PWC timer or input capture function has been selected. The pin cannot be set as the external count clock input pin when the PWC timer or input capture function has been selected.

To use this input feature, set the port direction register (DDR2:bit4) to "0" to set the pin as an input port.

#### EC01 internal pin:

This pin serves as the external count clock input pin for timer 01 when the interval timer or PWM timer function has been selected or the signal input pin for timer 01 when the PWC timer or input capture function has been selected. The pin cannot be set as the external count clock input pin when the PWC timer or input capture function has been selected.

This input is not used during 16-bit operation. The input can be used as well when the PWM timer function has been selected (variable-cycle mode).

To use this input feature, set the port direction register (DDR2:bit4) to set the pin as an input port.

## ■ Block Diagram of Pins Related to 8/16-bit Compound Timer



## Figure 15.4-1 Block Diagram of Pins (EC0) Related to 8/16-bit Compound Timer TO00 and TO01

## 15.5 Registers of 8/16-bit Compound Timer

## This section describes the registers related to the 8/16-bit compound timer.

## ■ Registers Related to 8/16-bit Compound Timer

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit0	bit0	Initial value	
0F92 <sub>H</sub> T01CR0	IFE	C2	C1	C0	F3	F2	F1	F0	00000000 <sub>B</sub>	
0F93 <sub>H</sub> T00CR0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	
8/16-bit compound timer 00/01 control status register 1 (T00CR1/T01CR1)										
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit0	bit0	Initial value	
0036 <sub>H</sub> T01CR1	STA	HO	IE	IR	BF	IF	SO	OE	00000000 <sub>B</sub>	
0037 <sub>H</sub> T00CR1	R/W	R/W	R/W	R(RM1),W	R/WX	R(RM1),W	R/W	R/W	2	
8/16-bit compound timer 00/01 data register (T00DR/T01DR)										
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit0	bit0	Initial value	
0F94 <sub>H</sub> T01DR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	00000000 <sub>B</sub>	
0F95 <sub>H</sub> T00DR	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	
8/16-bit compound timer 00/01 timer mode control register (TMCR0)										
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit0	bit0	Initial value	
0F96 <sub>H</sub> TMCR0	T01	T00	TIS	MOD	FE11	FE10	FE01	FE00	00000000 <sub>B</sub>	
	R/WX	R/WX	R/W	R/W	R/W	R/W	R/W	R/W		
R/W : Readable/writable (Read value is the same as write value)										
R(RM1),W : Readable/writable (Read value is different from write value, "1" is read by read-modify- write (RMW) instruction)										

#### Figure 15.5-1 Registers Related to 8/16-bit Compound Timer

## 15.5.1 8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0)

The 8/16-bit compound timer 00/01 control status register 0 (T00CR0/T01CR0) selects the timer operation mode, selects the count clock, and enables or disables IF flag interrupts. The T00CR0 and T01CR0 registers correspond to timers 00 and 01, respectively.

## ■ 8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0)

OF92H T01CR0 0F93H T00CR0         IFE         C2         C1         C0         F3         F2         F1         F0         00000000B           R/W         R/W
0F93H TOOCRO       R/W       R/W       R/W       R/W       R/W       R/W       R/W         F3       F2       F1       F0       Timer operation mode select bits         0       0       0       0       Interval timer (one-shot mode)         0       0       0       1       Interval timer (continuous mode)         0       0       1       0       Interval timer (free-run mode)         0       0       1       1       PWM timer (fixed-cycle mode)         0       1       0       1       PWC timer ("H" pulse = rising to falling)         0       1       0       1       PWC timer (cycle = rising to rising)         0       1       1       1       PWC timer (cycle = falling to falling)         0       1       1       1       PWC timer ("H" pulse = rising to falling)         1       0       0       1       1       PWC timer (cycle = falling to falling)         1       0       1       0       1       1       Input capture (rising, free-run counter)
F3F2F1F0Timer operation mode select bits0000Interval timer (one-shot mode)0001Interval timer (continuous mode)0010Interval timer (free-run mode)0011PWM timer (fixed-cycle mode)0110PWM timer (fixed-cycle mode)0101PWC timer ("H" pulse = rising to falling)0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)0111PWC timer (cycle = rising to falling)1001PWC timer (run cycle = rising to falling)101011010Input capture (rising, free-run counter)1011Input capture (falling, free-run counter)
F3F2F1F0Timer operation mode select bits0000Interval timer (one-shot mode)0001Interval timer (continuous mode)0010Interval timer (free-run mode)0011PWM timer (free-run mode)0011PWM timer (variable-cycle mode)010010101PWC timer ("H" pulse = rising to falling)0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)0111PWC timer (cycle = falling to falling)1001PWC timer (rycle = rising to falling)1010Input capture (rising, free-run counter)1011Input capture (falling, free-run counter)1011Input capture (falling, free-run counter)
F3F2F1F0Timer operation mode select bits0000Interval timer (one-shot mode)0001Interval timer (continuous mode)0010Interval timer (free-run mode)0011PWM timer (fixed-cycle mode)0100140100PWM timer (variable-cycle mode)01010101011PWC timer ("H" pulse = rising to falling)0110011PWC timer (cycle = rising to rising)0111001PWC timer (cycle = falling to rising)100110101011101110111001
F3F2F1F0Timer operation mode select bits0000Interval timer (one-shot mode)0001Interval timer (continuous mode)0010Interval timer (free-run mode)0011PWM timer (free-run mode)0011PWM timer (variable-cycle mode)0101PWC timer ("H" pulse = rising to falling)0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)0111PWC timer (cycle = falling to rising)1001PWC timer (rycle = falling to falling)1011Input capture (rising, free-run counter)1011Input capture (rising, free-run counter)1011Input capture (falling, free-run counter)
F3F2F1F0Timer operation mode select bits0000Interval timer (one-shot mode)0001Interval timer (continuous mode)0010Interval timer (free-run mode)0011PWM timer (free-run mode)0011PWM timer (variable-cycle mode)0101PWC timer ("H" pulse = rising to falling)0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)0111PWC timer (cycle = rising to falling)1001PWC timer (rycle = rising to falling)1011Input capture (rising, free-run counter)1011Input capture (rising, free-run counter)
0         0         0         0         Interval timer (one-shot mode)           0         0         0         1         Interval timer (continuous mode)           0         0         1         0         Interval timer (free-run mode)           0         0         1         0         Interval timer (free-run mode)           0         0         1         1         PWM timer (free-run mode)           0         0         1         1         PWM timer (free-run mode)           0         1         0         1         PWM timer (free-run mode)           0         1         0         0         PWM timer (free-run mode)           0         1         0         PWM timer (free-run mode)           0         1         0         PWM timer (run able-cycle mode)           0         1         0         PWC timer (run able-cycle mode)           0         1         0         PWC timer ("L" pulse = rising to falling)           0         1         1         PWC timer (run able-cycle mode)           1         0         1         PWC timer (cycle = rising to rising)           1         0         0         PWC timer (cycle = rising to falling)           1
0         0         1         Interval timer (continuous mode)           0         0         1         0         Interval timer (free-run mode)           0         0         1         1         PWM timer (fixed-cycle mode)           0         1         0         1         PWM timer (variable-cycle mode)           0         1         0         1         PWC timer ("H" pulse = rising to falling)           0         1         0         1         PWC timer ("L" pulse = falling to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           1         0         0         1         PWC timer (cycle = falling to falling)           1         0         0         1         PWC timer (cycle = rising to falling)           1         0         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         0         Input capture (rising, free-run counter)           1         0         1         1         Input capture (falling, free-run counter)
0         0         1         0         Interval timer (free-run mode)           0         0         1         1         PWM timer (fixed-cycle mode)           0         1         0         0         PWM timer (variable-cycle mode)           0         1         0         0         PWC timer (variable-cycle mode)           0         1         0         1         PWC timer ("H" pulse = rising to falling)           0         1         1         0         PWC timer ("L" pulse = falling to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           1         0         0         1         PWC timer (cycle = falling to falling)           1         0         0         1         PWC timer (cycle = falling to falling)           1         0         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         0         Input capture (rising, free-run counter)           1         0         1         1         Input capture (falling, free-run counter)
0         0         1         1         PWM timer (fixed-cycle mode)           0         1         0         0         PWM timer (variable-cycle mode)           0         1         0         1         PWC timer (variable-cycle mode)           0         1         0         1         PWC timer ("H" pulse = rising to falling)           0         1         1         0         PWC timer ("L" pulse = falling to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           1         0         0         0         PWC timer (cycle = falling to falling)           1         0         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         O         Input capture (rising, free-run counter)           1         0         1         1         Input capture (falling, free-run counter)
0         1         0         0         PWM timer (variable-cycle mode)           0         1         0         1         PWC timer ("H" pulse = rising to falling)           0         1         1         0         PWC timer ("L" pulse = falling to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           0         1         1         1         PWC timer (cycle = rising to rising)           1         0         0         0         PWC timer (cycle = falling to falling)           1         0         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         PWC timer ("H" pulse = rising to falling)           1         0         1         Input capture (rising, free-run counter)           1         0         1         1         Input capture (falling, free-run counter)
0101PWC timer ("H" pulse = rising to falling)0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)1000PWC timer (cycle = falling to falling)1001PWC timer ("H" pulse = rising to falling)101PWC timer ("H" pulse = rising to falling; Cycle = rising to rising)1010101Input capture (rising, free-run counter)10111000
0110PWC timer ("L" pulse = falling to rising)0111PWC timer (cycle = rising to rising)1000PWC timer (cycle = falling to falling)1001PWC timer ("H" pulse = rising to falling; Cycle = rising to rising)101011010Input capture (rising, free-run counter)1011Input capture (falling, free-run counter)11000
011PWC timer (cycle = rising to rising)100PWC timer (cycle = falling to falling)1001PWC timer ("H" pulse = rising to falling; Cycle = rising to risin1010Input capture (rising, free-run counter)1011Input capture (falling, free-run counter)1011Input capture (falling, free-run counter)
1       0       0       PWC timer (cycle = falling to falling)         1       0       0       1       PWC timer ("H" pulse = rising to falling; Cycle = rising to risin         1       0       1       0       Input capture (rising, free-run counter)         1       0       1       1       Input capture (falling, free-run counter)         1       0       1       1       Input capture (falling, free-run counter)
1     0     1     PWC timer ("H" pulse = rising to falling; Cycle = rising to risin       1     0     1     0     Input capture (rising, free-run counter)       1     0     1     1     Input capture (falling, free-run counter)       1     0     1     1     Input capture (falling, free-run counter)
1     0     1     0     Input capture (rising, free-run counter)       1     0     1     1     Input capture (falling, free-run counter)       1     1     0     0     Input capture (bath addas, free-run counter)
1 0 1 1 Input capture (falling, free-run counter)
1 1 0 0 Input capture (both edges free-rup counter)
1 1 0 1 Input capture (rising, counter clear)
1 1 1 0 Input capture (falling, counter clear)
1 1 1 Input capture (both edges, counter clear)
C2 C1 C0 Count clock select bits
0 0 0 1 x MCLK (machine clock)
0 0 1 1/2 x MCLK (machine clock)
0 1 0 1/4 x MCLK (machine clock)
0 1 1 1/8 x MCLK (machine clock)
1 0 0 1/16 x MCLK (machine clock)
1 0 1 1/32 x MCLK (machine clock)
1 1 0 1/2 <sup>7</sup> х Fсн
1 1 1 External clock
IFE IF flag interrupt enable
IF flag interrupt disabled
1   IF flag interrupt enabled
R/W : Readable/writable (Read value is the same as write value)

Figure 15.5-2 8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0)

## Table 15.5-1 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0) (1 / 2)

bit7 IFE: Set IF flag interrupt enable Set	is bit enab t <b>ting this l</b> t <b>ting this</b>	les or disa bit to ''0'	ables IF fl	ag interrupts.		
	This bit enables or disables IF flag interrupts. Setting this bit to "0": disables IF flag interrupts. Setting this bit to "1": an IF flag interrupt request is outputted when both the IE bit (T00 T01CR1:IE) and the IF flag (T00CR1/T01CR1:IF) are set to "1".					
bit6 to bit4 C2, C1, C0: Count clock select bits	ese bits se. The count of Vrite access The clock s These bits of vrite "1111 <sub>H</sub> lso reset to C2 0 0 0 0 1 1 1 1	lect the co clock is gest to these selection of cannot be $B^{*}$ with the $D^{*}OOO_{B}^{*}$ is C1 0 1 1 0 0 1 1 1 0 1 1 1 1 1 1 1 1 1 1	ount clock enerated b e bits is nu of T01CR set to "11 e PWC or if the time CO 0 1 0 1 0 1 0 1 0 1	by the prescaler. Refer to "6.12 Operating Explanation of illified during timer operation (T00CR1/T01CR1:STA = 100 (timer 01) is nullified during 16-bit operation. 11 <sub>B</sub> " when the PWC or input capture function is used. An r input capture function in use resets the bits to "000 <sub>B</sub> ". The r enters the input capture operation mode with the bits set Count clock select bits $1 \times MCLK$ (machine clock) $1/2 \times MCLK$ (machine clock) $1/4 \times MCLK$ (machine clock) $1/8 \times MCLK$ (machine clock) $1/16 \times MCLK$ (machine clock) $1/32 \times MCLK$ (machine clock) $1/32 \times MCLK$ (machine clock) $1/2^7 \times F_{CH}$ External clock	Prescaler". 1). a attempt to The bits are t to "111 <sub>B</sub> ".	

## Table 15.5-1 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0) (2 / 2)

Bit name		Function								
		These bits select the timer operation mode. • The PWM timer function (variable-cycle mode; F3, F2, F1, F0 = $0100_B$ ) is set by either the T00CR0 (timer 00) register or T01CR0 (timer 01) register. In this case, the other register is set to F3, F2, F1, F0 = $0100_B$ automatically when the timer starts operation (T00CR1/T01CR1: STA= 1). • The MOD bit is set to "0" automatically when the timer set for 16-bit operation (TMCR0:MOD = 1) starts operation (T00CR1/T01CR1:STA = 1) in the PWM timer function (variable-cycle mode). • Write access to these bits is nullified during timer operation (T00CR1/T01CR1:STA = 1).								
			F3	F2	F1	F0	Timer operation mode select bits			
			0	0	0	0	Interval timer (one-shot mode)			
			0	0	0	1	Interval timer (continuous mode)			
			0	0	1	0	Interval timer (free-run mode)			
bit3 F3, F2, F1, F to Timer operat bit0 select bits			0	0	1	1	PWM timer (fixed-cycle mode)			
			0	1	0	0	PWM timer (variable-cycle mode)			
	F3, F2, F1, F0: Timer operation mode select bits		0	1	0	1	PWC timer ("H" pulse = rising to falling)			
			0	1	1	0	PWC timer ("L" pulse = falling to rising)			
			0	1	1	1	PWC timer (cycle = rising to falling)			
			1	0	0	0	PWC timer (cycle = falling to rising)			
			1	0	0	1	PWC timer ("H" pulse = rising to falling; Cycle = rising to rising)			
			1	0	1	0	Input capture (rising, free-run counter)			
			1	0	1	1	Input capture (falling, free-run counter)			
			1	1	0	0	Input capture (both edges, free-run counter)			
			1	1	0	1	Input capture (rising, counter clear)			
			1	1	1	0	Input capture (falling, counter clear)			
			1	1	1	1	Input capture (both edges, counter clear)			

## 15.5.2 8/16-bit Compound Timer 00/01 Control Status Register 1 (T00CR1/T01CR1)

8/16-bit compound timer 00/01 control status register 1 (T00CR1/T01CR1) controls the interrupt flag, timer output, and timer operations. T00CR1 and T01CR1 registers correspond to timers 00 and 01, respectively.

## ■ 8/16-bit Compound Timer 00/01 Control Status Register 1 (T00CR1/T01CR1)



Figure 15.5-3 8/16-bit Compound Timer 00/01 Control Status Register 1 (T00CR1/T01CR1)
	Bit name	Function
bit7	STA: Timer operation enable bit	<ul> <li>This bit enables or stops timer operation.</li> <li>Writing "0": stops the timer operation and sets the count value to "00<sub>H</sub>".</li> <li>When the PWM timer function (variable-cycle mode) has been selected (T00CR0/T01CR0: F3, F2, F1, F0 = 0100<sub>B</sub>), the STA bit can be used to enable or disable timer operation from within either the T00CR1 (timer 00) or T01CR1 (timer 01) register. In this case, the STA bit in the other register is set to the same value automatically.</li> <li>During 16-bit operation (TMCR0:MD = 1), use the STA bit in the T00CR1 (timer 00) register to enable or disable timer operation. In this case, the STA bit in the other register is set to the same value automatically.</li> <li>Writing "1": allows timer operation to start from count value "00<sub>H</sub>".</li> <li>Set this bit to "1" after setting the count clock select bits (T00CR0/T01CR0:C2, C1, C0), timer operation select bits (T00CR0/T01CR0:F3, F2, F1, F0), timer output initial value bit (T00CR1/T01CR1:SO), 16-bit mode enable bit (TMCR0:MD), and filter function select bits (TMCR0:FE11, FE10, FE01, FE00).</li> </ul>
bit6	HO: Timer suspend bit	<ul> <li>This bit suspends or resumes timer operation.</li> <li>Writing "1" to this bit during timer operation suspends the timer operation.</li> <li>Writing "0" to the bit when timer operation has been enabled (T00CR1/T01CR1:STA = 1) resumes the timer operation.</li> <li>When the PWM timer function (variable-cycle mode) has been selected (T00CR0/T01CR0: F3, F2, F1, F0=0100<sub>B</sub>), the HO bit can be used to suspend or resume timer operation from within either the T00CR1 (timer 00) or T01CR1 (timer 01) register. In this case, the HO bit in the other register is set to the same value automatically.</li> <li>During 16-bit operation (TMCR0:MD = 1), use the HO bit in the other register is set to the same value automatically.</li> </ul>
bit5	IE: Interrupt request enable bit	This bit enables or disables the output of interrupt requests.         Writing "0": disables interrupt request.         Writing "1": outputs an interrupt request when the pulse width measurement completion/edge detection flag (T00CR1/T01CR1:IR) or timer reload/overflow flag (T00CR1/T01CR1:IF) is "1".         Note, however, that an interrupt request from the timer reload/overflow flag (T00CR1/T01CR1:IF) is not outputted unless the IF flag interrupt enable (T00CR0/T01CR0:IFE) bit is also set to "1".
bit4	IR: Pulse width measurement completion/edge detection flag	<ul> <li>This bit shows the completion of pulse width measurement or the detection of an edge.</li> <li>The bit is set to "1" upon completion of pulse width measurement when the PWC timer function has been selected.</li> <li>The bit is set to "1" upon detection of an edge when the input capture function has been selected.</li> <li>The bit is "0" when any timer function other than the PWC timer and input capture functions has been selected.</li> <li>This bit always returns "1" to a read modify write (RMW) instruction.</li> <li>The IR bit in T01CR1 (timer 01) register is set to "0" during 16-bit operation.</li> <li>Writing "0" to the bit sets it to "0".</li> <li>An attempt to write "1" to the bit is ignored.</li> </ul>

## Table 15.5-2 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Control Status Register 1 (1 / 2)

	Bit name	Function
bit3	BF: Data register full flag	<ul> <li>This bit is set to "1" when a count value is stored in the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) upon completion of pulse width measurement in PWC timer function.</li> <li>This bit is set to "0" when the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is read during 8-bit operation.</li> <li>The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) holds data with this bit containing "1". Even when the next edge is detected with this bit containing "1", the count value is not transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) and thus the next measurement result is lost. However, as the exception, when the "H" pulse and cycle measurement (T00CR0/T01CR0: F3, F2, F1, F0= 1001<sub>B</sub>) is selected, the "H" pulse measurement result is transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) with this bit set to "1". The cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) with this bit set to "1". The cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) with this bit set to "1". The cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) with this bit set to "1". The cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) with this bit set to "1". The cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register with the bit set to "1". For cycle measurement, therefore, the "H" pulse measurement result must be read before the cycle is completed. Note also that the result of "H" pulse.</li> <li>The BF bit in the T00CR1 (timer 00) register is set to "0" when the T01DR (timer 01) register is read during 16-bit operation.</li> <li>The BF bit in T01CR1 (timer 01) register is set to "0" during 16-bit operation.</li> <li>This bit is "0" when any timer function other than the PWC timer function</li></ul>
bit2	IF: Timer reload/overflow flag	<ul> <li>This bit detects a match with a count value or a counter overflow.</li> <li>The bit is set to "1" when the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) value matches the count value during interval timer function (both one-shot and continuous mode) or PWM timer function (variable-cycle mode).</li> <li>The bit is set to "1" when a counter overflow occurs during PWC or input capture function.</li> <li>This bit always returns "1" to a read-modify-write (RMW) instruction.</li> <li>Writing "0" to the bit sets it to "0".</li> <li>Writing "1" to this bit has no effects on the operation.</li> <li>The bit is "0" when the PWM function (variable-cycle mode) has been selected.</li> <li>The IF bit in the T01CR1 (timer 01) register is "0" during 16-bit operation.</li> </ul>
bit1	SO: Timer output initial value bit	<ul> <li>Writing to this bit sets the timer output (TMCR0:TO1/TO0) initial value. The value in this bit is reflected in the timer output when the timer operation enable bit (T00CR1/T01CR1:STA) changes from "0" to "1".</li> <li>During 16-bit operation (TMCR0:MOD = 1), use the SO bit in the T00CR1 (timer 00) register to set the timer output initial value. In this case, the value of the S bit in the other register is meaningless.</li> <li>An attempt to write to this bit is nullified during timer operation (T00CR1/T01CR1:STA = 1). During 16-bit operation, however, a value can be written to the SO bit in the T01CR1 (timer 01) register even during timer operation but it has no direct effect on the timer output.</li> <li>The value of this bit is meaningless when the PWM timer function (either fixed-cycle or variable-cycle mode) or input capture function has been selected.</li> </ul>
bit0	OE: Timer output enable bit	<ul> <li>This bit enables or disabled timer output.</li> <li>Writing "0": prevents the timer output from being supplied to the external pin. In this case, the external pin serves as a general-purpose port.</li> <li>Writing "1": supplies timer output (TMCR0:TO1/TO0) to the external pin.</li> </ul>

## Table 15.5-2 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Control Status Register 1 (2 / 2)

## 15.5.3 8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0)

The 8/16-bit compound timer 00/01 timer mode control register ch.0 (TMCR0) selects the filter function, 8-bit or 16-bit operation mode, and signal input to timer 00 and to indicate the timer output value. This register serves for both of timers 00 and 01.

■ 8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0)

TMCR0 Address 0F96н	bit7     bit6     bit5     bit4     bit3     bit2     bit1     bit0     Initial value       TO1     TO0     IIS     MOD     FE11     FE10     FE01     FE00     00000000 <sub>B</sub> R/WX     R/W     R/W     R/W     R/W     R/W     R/W
	FE01 FE00 Timer 00 filter function select bits
	0 1 Removing "H" pulse noise
	1 0 Removing "L" pulse noise
	1 1 Removing "H"/"L" pulse noise
	FE11   FE10   Timer 01 filter function select bits
	0 0 No filtering
	0 1 Removing "H" pulse noise
	1 0 Removing "L" pulse noise
	1 1 Removing "H"/"L" pulse noise
	MOD 8-bit/16-bit operation mode select bit
	0 8-bit operation
	1 16-bit operation
	IIS Timer 00 internal signal select bit
	0 Selecting external signal (EC00) as timer 00 input
	Selecting internal signal (110) as timer 00 input
	Output value of timer 00
	TO1 Timer 01 output bit
	Output value of timer 01
R/W : R R(RM1),W : R R/WX : R	Readable/writable (Read value is the same as write value) Readable/writable (Read value is different from write value, "1" is read by read-modify-write (RMW) instruction) Read only (Readable, writing has no effect on operation) itial value

Figure 15.5-4 8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0)

## Table 15.5-3 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0) (1 / 2)

	Bit name				Function			
bit7	TO1: Timer 01 output bit	<ul> <li>This bit indicates the output value of timer 01. When the timer starts operation (100CR1/T01CR1:STA = 1), the value in the bit changes depending on the selected timer function.</li> <li>Writing to this bit has no effect on the operation.</li> <li>The value in the bit remains indeterminate during 16-bit operation when the PWM timer function (variable-cycle mode) or input capture function has been selected.</li> <li>When the timer stops operation (T00CR1/T01CR1:STA = 0) in interval timer or PWC timer function, this bit holds the last value.</li> <li>When the timer stops operation in PWM timer function (fixed-cycle mode), this bit holds the last value.</li> <li>When the timer operation mode select bit (T00CR0/T01CR0: F3, F2, F1, F0) is changed with the timer being stopped, the bit indicates the last value of timer operation if the same timer operation has ever been performed or otherwise contains "0".</li> </ul>						
bit6	TO0: Timer 00 output bit	<ul> <li>This bit indicates the output value of timer 00. When the timer starts operation (T00CR1/T01CR1:STA = 1), the value in the bit changes depending on the selected timer function.</li> <li>Writing to this bit has no effect on the operation.</li> <li>The value in the bit remains indeterminate when the input capture function has been selected.</li> <li>When the timer stops operation (T00CR1/T01CR1:STA = 0) in interval timer, PWM timer (variable-cycle mode), or PWC timer function, this bit holds the last value.</li> <li>When the timer stops operation in PWM timer function (fixed-cycle mode), this bit holds the last value.</li> <li>When the timer operation mode select bit (T00CR0/T01CR0: F3, F2, F1, F0) is changed with the timer being stopped, the bit indicates the last value of timer operation if the same timer operation has ever been performed or otherwise contains "0".</li> </ul>						
bit5	IIS: Timer 00 internal signal select bit	Th sel Wi Wi	is bit sele ected. riting ''0' riting ''1'	cts the sig ': selects t ': selects t	nal input to timer 00 when the PWC timer or input capture f he external signal (EC00) as the signal input for timer 00. he internal signal (TII0) as the signal input for timer 00.	unction has been		
bit4	MOD: 16-bit mode enable bit	Th W1 W1 • 7 F • V	is bit select riting ''0' riting ''1' This bit is PWM time Write acce	cts 8-bit of ': allows t ': allows t set to "0" er mode (v ess to this l	r 16-bit operation mode. imers 00 and 01 to operate as separate 8-bit timers. imers 00 and 01 to operate as a 16-bit timer. ' automatically when the timer starts operation (T00CR1/T0 variable-cycle mode). bit is nullified during timer operation (T00CR1:STA = 1 or T0	1CR1:STA=1) in 01CR1:STA = 1).		
		Th or	ese bits so input capt	elect the fi ure function	ilter function for the external signal (EC01) to timer 01 when on has been selected.	n the PWC timer		
			FE11	FE10	Timer 01 filter function select bits			
	EE11 EE10.		0	0	No filtering			
bit3	Timer 01 filter function		0	1	Removing "H" pulse noise			
bit2	select bits		1	0	Removing "L" pulse noise			
			1	1	Removing "H"/"L" pulse noise			
		• \ • ] h	Write acce The setting as been se	ess to these gs of the b elected (fi	e bits is nullified during timer operation (T01CR1:STA = 1). its have no effect on operation when the interval timer or PW. Iter function does not operate.).	M timer function		

## Table 15.5-3 Functional Description of Each Bit of 8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0) (2 / 2)

	Bit name				Function					
		Th or	These bits select the filter function for the external signal (EC00) to timer 00 when the PWC t or input capture function has been selected.							
FE01 FE00 Timer 00 filter function select	Timer 00 filter function select bits									
	0 0 No filtering	No filtering								
bit1	FE01, FE00: Timer 00 filter function		0	1	Removing "H" pulse noise					
bit0	select bits		1	0	Removing "L" pulse noise					
			1	1	Removing "H"/"L" pulse noise					
		• / • ] f	An attemp The settin function h	ot to write t ags of thes as been sel	to these bits is nullified during timer operation (T00CR1:STA e bits have no effect on operation when the interval time lected (filter function does not operate.).	A = 1). er or PWM timer				

# 15.5.4 8/16-bit Compound Timer 00/01 Data Register ch.0 (T00DR/T01DR)

The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is used to write the maximum value counted during interval timer or PWM timer operation and to read the count value during PWC timer or input capture operation. The T00DR and T01DR registers correspond to timers 00 and 01, respectively.

### ■ 8/16-bit Compound Timer 00/01 Data Register (T00DR/T01DR)

### Figure 15.5-5 8/16-bit Compound Timer 00/01 Data Register (T00DR/T01DR)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	
0F94 <sub>H</sub> T01DR	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	00000000 <sub>B</sub>	
0F95 <sub>H</sub> T00DR	R/W									
R/W: Readable/writable (Read value is the same as write value)										

### Interval timer function

The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is used to set the interval time. When the timer starts operation (T00CR1/T01CR1:STA = 1), the value of this register is transferred to the latch in the 8-bit comparator and the counter starts counting. When the count value matches the value held in the latch in the 8-bit comparator, the value of this register is transferred again to the latch and the count value is reset to " $00_{\text{H}}$ " to continue to count.

The current count value can be read from this register.

An attempt to write " $00_{\text{H}}$ " to this register is disabled in interval timer function.

In 16-bit operation, set the upper data to T01DR and lower data to T00DR. And, write and read T01DR and T00DR in this order.

### PWM timer functions (fixed-cycle)

The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is used to set "H" pulse width time. When the timer starts operation (T00CR1/T01CR1:STA=1), the value of this register is transferred to the latch in the 8-bit comparator and the counter starts counting from timer output "H". When the count value matches the value held in the latch, the timer output becomes "L" and the counter continues to count until the count value reaches "FF<sub>H</sub>". When an overflow occurs, the value of this register is transferred again to the latch in the 8-bit comparator and the counter performs the next cycle of counting.

The current value can be read from this register. In 16-bit operation, set the upper data to T01DR and lower data to T00DR. And, write and read T01DR and T00DR in this order.

#### PWM timer functions (variable-cycle)

The 8/16-bit compound timer 00 data register (T00DR) and 8/16-bit compound timer 01 data register (T01DR) are used to set "L" pulse width timer and cycle, respectively. When the timer starts operation (T00CR1/T01CR1:STA = 1), the value of each register is transferred to the latch in the 8-bit comparator and two counters start counting from timer output "L". When the T00DR value held in the latch matches the timer 00 counter value, the timer output becomes "H" and the counting continues until the T01DR value held in the latch of the 8-bit comparator matches the timer 01 counter value. When the T01DR value held in the latch of the 8-bit comparator matches the timer 01 counter value, the values of these registers are transferred again to the latch and the next PWM cycle of counting is performed continuously.

The current count value can be read from this register.

In 16-bit operation, set the upper data and lower data to T01DR and T00DR, respectively. And, write and read T01DR and T00DR in this order.

#### PWC timer function

The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is used to read PWC measurement results. When PWC measurement is completed, the counter value is transferred to this register and the BF bit is set to "1".

When the 8/16-bit compound timer 00/01 data register is read, the BF bit is set to "0". Transfer to the 8/16-bit compound timer 00/01 data register is not performed with the BF bit containing "1".

As the exception, when the "H" pulse and cycle measurement (T00CR0/T01CR0:F3, F2, F1, F0 =  $1001_B$ ) is selected, the "H" pulse measurement result is transferred to the 8/16-bit compound timer 00/01 data register with the BF bit set to "1", but the cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register with the BF bit set to "1". For cycle measurement, therefore, the "H" pulse measurement result must be read before the cycle is completed. Note also that the result of "H" pulse measurement is lost unless read before the completion of the next "H" pulse.

When reading the 8/16-bit compound timer 00/01 data register, be careful not to clear the BF bit unintentionally.

Writing to the 8/16-bit compound timer 00/01 data register updates the stored measurement data with the write value. Therefore, do not perform a write operation. In 16-bit operation, the upper data and lower data are transferred to T01DR and T00DR, respectively. Read T01DR and T00DR in this order.

#### Input capture function

The 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is used to read input capture results. When a specified edge is detected, the counter value is transferred to the 8/16-bit compound timer 00/01 data register.

Writing a value to the data register updates the measurement data stored there with that value. Therefore, do not write to the 8/16-bit compound timer 00/01 data register. In 16-bit operation, the upper data and lower data are transferred to T01DR and T00DR, respectively. Read T01DR and T00DR in this order.

### Read and write operations

Read and write operations of T00DR and T01DR are performed in the following manner during 16-bit operation and PWM timer function (variable-cycle).

- Read from T01DR: Read access from the register also involves storing the T00DR value into the internal read buffer.
- Read from TOODR: Read from the internal read buffer.
- Write to T01DR: Write to the internal write buffer.
- Write to T00DR: Write access to the register also involves storing the value of the internal write buffer into T01DR.

Figure 15.5-6 shows the T00DR and T01DR registers read from and written to during 16-bit operation.

#### Figure 15.5-6 T00DR and T01DR registers read from and written to during 16-bit operation



### 15.6 Interrupts of 8/16-bit Compound Timer

## The 8/16-bit compound timer generates the following types of interrupts to each of which an interrupt number and interrupt vector are assigned.

- Timer 00 interrupt
- Timer 01 interrupt

### ■ Timer 00 Interrupt

Table 15.6-1 explains the timer 00 interrupt and its source.

Table 15.6-1 Timer 00 Interrupt

ltem		Description	
Interrupt generating condition	Comparison match in interval timer function or PWM timer function (variable-cycle mode) has been selected	Overflow in PWC timer function or input capture function	Completion of measurement in PWC timer function or edge detection in input capture function
Interrupt flag	T00CR1:IF	T00CR1:IF	T00CR1:IR
Interrupt enable	T00CR1:IE and T00CR0:IFE	T00CR1:IE and T00CR0:IFE	T00CR1:IE

### ■ Timer 01 Interrupt

Table 15.6-2 explains the timer 01 interrupt and its cause.

### Table 15.6-2 Timer 01 Interrupt

ltem		Description	
Interrupt generating condition	Comparison match in interval timer function or PWM timer function (variable-cycle mode) has been selected Excluded during 16-bit operation	Overflow in PWC timer function or input capture function Excluded during 16-bit operation	Completion of measurement in PWC timer function or edge detection in input capture function Excluded during 16-bit operation
Interrupt flag	T01CR1:IF	T01CR1:IF	T01CR1:IR
Interrupt enable	T01CR1:IE and T00CR0:IFE	T01CR1:IE and T00CR0:IFE	T01CR1:IE

### ■ Registers and Vector Tables Related to Interrupts of 8/16-bit Compound Timer

Interrupt	Interrupt	Interrupt level	setup register	Vector table address		
source	request No.	Register	Setting bit	g bit Upper Lower	Lower	
Timer 00	IRQ5	ILR1	L05	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	
Timer 01	IRQ6	ILR1	L06	FFEE <sub>H</sub>	FFEF <sub>H</sub>	

Table 15.6-3 Registers and Vector Tables Related to Interrupts of 8/16-bit Compound Timer

The request numbers and vector tables of all peripheral functions are listed in Appendix B "Interrupt Source Tables".

## 15.7 Operating Description of Interval Timer Function (Oneshot Mode)

This section describes the operations of the interval timer function (one-shot mode) for the 8/16-bit compound timer.

### Operation of Interval Timer Function (One-shot Mode)

The compound timer requires the register settings shown in Figure 15.7-1 to serve as the interval timer function.



Figure 15.7-1 Settings of Interval Timer Function

In interval timer function (one-shot mode), enabling timer operation (T00CR0/T00CR1:STA = 1) causes the counter to start counting from " $00_{\text{H}}$ " at the rising edge of a selected count clock signal. When the counter value matches the value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR), the timer output (TMCR0:T00/T01) is inverted, the interrupt flag (T00CR1/T01CR1:IF) is set to "1" and the start bit (T00CR0/T00CR1:STA) is set to "0", and then the count operation stops.

The value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is transferred to the temporary storage latch (comparison data storage latch) in the comparator when the counter starts counting. Writing " $00_{\text{H}}$ " to the 8/16-bit compound timer 00/01 data register is prohibited.

Figure 15.7-2 shows the operation of the interval timer function in the 8-bit operation.



Figure 15.7-2 Operation of Interval Timer Function in 8-bit Mode (Timer 0)

## 15.8 Operating Description of Interval Timer Function (Continuous Mode)

## This section describes the interval timer function (continuous mode operation) of the 8/16-bit compound timer.

### Operation of Interval Timer Function (Continuous Mode)

The compound timer requires the register settings shown in Figure 15.8-1 to serve as the interval timer function (continuous mode).



### Figure 15.8-1 Settings for Counter Function (8-bit Mode)

In interval timer function (continuous mode), enabling timer operation (T00CR0/T00CR1:STA = 1) causes the counter to start counting from " $00_{\text{H}}$ " at the rising edge of a selected count clock signal. When the counter value matches the value in the 8/16-bit compound timer 00/01 data register (T00DR/T01DR), the timer output bit (TMCR0:T00/T01) is inverted, the interrupt flag (T00CR1/T01CR1:IF) is set to "1", and the counter continues to count by restarting at " $00_{\text{H}}$ ". The timer outputs a square wave as a result of this continuous operation.

The value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is transferred to the temporary storage latch (comparison data storage latch) in the comparator either when the counter starts counting or when a counter value comparison match is detected. Writing " $00_{\rm H}$ " to the 8/16-bit compound timer 00/01 data register is disabled during the count operation.

When the timer stops operation, the timer output bit (TMCR0:TO0/TO1) holds the last value.



### Figure 15.8-2 Operating Diagram of Interval Timer Function (Continuous Mode)

# 15.9 Operating Description of Interval Timer Function (Free-run Mode)

## This section describes the operation of the interval timer function (free-run mode) for the 8/16-bit compound timer.

### Operation of Interval Timer Function (Free-run Mode)

The compound timer requires the settings shown in Figure 15.9-1 to serve as the interval timer function (free-run mode).



### Figure 15.9-1 Settings for Interval Timer Function (Free-run Mode)

In interval timer function (free-run mode), enabling timer operation (T00CR0/T00CR1:STA = 1) causes the counter to start counting from " $00_{\text{H}}$ " at the rising edge of a selected count clock signal. When the counter value matches the value in the 8/16-bit compound timer 00/01 data register (T00DR/T01DR), the timer output bit (TMCR0:T00/T01) is inverted and the interrupt flag (T00CR1/T01CR1:IF) is set to "1". The counter continues to count, and when the count value reaches "FF<sub>H</sub>", it restarts counting at " $00_{\text{H}}$ " to continue. The timer outputs a square wave as a result of this continuous operation.

The value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is transferred to the temporary storage latch (comparison data storage latch) in the comparator either when the counter starts counting or when a counter value comparison match is detected. Writing " $00_{\rm H}$ " to the 8/16-bit compound timer 00/01 data register is prohibited.

When the timer stops operation, the timer output bit (TMCR0:TO0/TO1) holds the last value.



Figure 15.9-2 Operating Diagram of Interval Timer Function (Free-run Mode)

# 15.10 Operating Description of PWM Timer Function (Fixed-cycle mode)

## This section describes the operation of the PWM timer function (fixed-cycle mode) for the 8/16-bit compound timer.

### Operation of PWM Timer Function (Fixed-cycle Mode)

The compound timer requires the settings shown in Figure 15.10-1 to serve as the PWM timer function (fixed-cycle mode).



#### Figure 15.10-1 Settings for PWM Timer Function (Fixed-cycle Mode)

In PWM timer function (fixed-cycle mode), a fixed cycle PWM signal in a variable "H" pulse width is outputted from the timer output pin (TO00/TO01). The cycle is fixed to " $FF_H$ " in 8-bit operation or " $FFFF_H$ " in 16-bit operation. The time is determined by the count clock selected. The "H" pulse width is specified by the value in the 8/16-bit compound timer 00/01 data register (T00DR/T01DR).

This function has no effect on the interrupt flag (T00CR1/T01CR1:IF). As each cycle always starts with "H" pulse output, the timer output initial value setting bit (T00CR1/T01CR1:SO) is meaningless.

The value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is transferred to the temporary storage latch (comparison data storage latch) in the comparator either when the counter starts counting or when a counter value comparison match is detected.

When the timer stops operation, the timer output bit (TMCR0:TO0/TO1) holds the last value.

The "H" pulse is one count clock shorter than the setting value in the output waveform immediately after activation of the timer (write "1" to the STA bit).

<u> </u>	5	
T00DR/T01DR register value: "00 <sub>H</sub> " (du	ty ratio = 0%)	
Counter value	00 <sub>H</sub>	→ FFH00 <sub>H</sub> →
PWM waveform "H" "L"-		
T00DR/T01DR register value: "80 <sub>H</sub> " (dut	ty ratio = 50%)	
Counter value	00 <sub>H</sub> → 80 <sub>H</sub>	FFH00 <sub>H</sub> >
"H" PWM waveform "L"-	ji	
T00DR/T01DR register value: "FF $_{H}$ " (du	ity ratio = 99.6%)	
Counter value "H PWM waveform "L'	0 <u>0</u> н ————————————————————————————————————	→ FFH00 <sub>H</sub> → One count width
Note: When the PWM function has (T00CR0/T01CR0:STA = 0).	been selected, the timer output pin holds the lev	vel used when the counter stops

### Figure 15.10-2 Operating Diagram of PWM Timer Function (Fixed-cycle Mode)

## 15.11 Operating Description of PWM Timer Function (Variablecycle Mode)

This section describes the operations of the PWM timer function (variable-cycle mode) for the 8/16-bit compound timer.

### ■ Operation of PWM Timer Function (Variable-cycle Mode)

The compound timer requires the settings shown in Figure 15.11-1 to serve as the PWM timer function (variable-cycle mode).

	U		<u> </u>						/	
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
то	0CR0/T01CR0	IFE	C2	C1	C0	F3	F2	F1	F0	
		О	О	О	О	0	1	0	0	
ТО	0CR1/T01CR1	STA	HO	IE	IR	BF	IF	SO	OE	
		1	О	О	×	×	О	×	×	
	TMCR	TO1	TO0	IIS	MOD	FE11	FE10	FE01	FE00	
		О	О	×	×	О	О	О	О	
	T00DR			Sets "L"	pulse widt	h (compar	e value)			
	T01DR		Sets the cycle of PWM waveform (compare value)							
	•	O: Used b	O: Used bit							
		x: Unused	x: Unused bit							
		1: Set "1"								

Figure 15.11-1 Settings for PWM Timer Function (Variable-cycle Mode)

In PWM timer function (variable-cycle mode), both timers 00 and 01 are used when the cycle is specified by the 8/16-bit compound timer 01 data register (T01DR), and the "L" pulse width is specified by the 8/16-bit compound timer 00 data register (T00DR), any cycle and duty PWM signal is generated from the timer output bit (T000).

For this function, the compound timer cannot serve as a 16-bit counter as the two 8-bit counters are used.

Enabling timer operation (by setting either T00CR1:STA = 1 or T01CR1:STA = 1) sets the mode bit (TMCR0:MOD) to "0". As the first cycle always begins with "L" pulse output, the timer initial value setting bit (T00CR1/T01CR1:SO) is meaningless.

The interrupt flag (T00CR1/T01CR1:IF) is set when each 8-bit counter matches the value in the corresponding 8/16-bit compound timer 00/01 data register (T00DR/T01DR).

The 8/16-bit compound timer 00/01 data register value is transferred to the temporary storage latch (comparison data storage latch) in the comparator either when the counter starts counting or when a comparison match with each counter value is detected.

"H" is not outputted when the "L" pulse width setting value is greater than the cycle setting value.

The count clock must be selected for both of timers 00 and 01. Selecting different count clocks, however, is prohibited.

When the timer stops operation, the timer output bit (TMCR0:TO0) holds the last output value.

If the 8/16-bit compound timer 00/01 data register is written over during operation, the written data will be effective from the cycle immediately after the detection of a synchronous match.



### Figure 15.11-2 Operating Diagram of PWM Timer Function (Variable-cycle Mode)

### 15.12 Operating Description of PWC Timer Function

## This section describes the operations of the PWC timer function for the 8/16-bit compound timer.

### Operation of PWC Timer Function

The compound timer requires the settings shown in Figure 15.12-1 to serve as the PWC timer function.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
T00CR0/T01CR0	IFE	C2	C1	C0	F3	F2	F1	F0
	О	О	О	О	О	О	О	0
T00CR1/T01CR1	STA	HO	IE	IR	BF	IF	SO	OE
	1	О	О	О	О	О	О	×
TMCR	TO1	TO0	IIS	MOD	FE11	FE10	FE01	FE00
	О	О	О	О	О	О	О	0
T00DR/T01DR			Holds pu	lse width r	neasurem	ent value		
	O: Used b	it						
	x: Unused	bit						
	1: Set "1"							

Figure 15.12-1 Settings for PWC Timer Function

When the PWC timer function is selected, the width and cycle of an external input pulse can be measured. The edges to start and end counting are selected by timer operation mode setting (T00CR0/T01CR0:F3, F2, F1, F0).

In this operation mode, the counter starts counting from " $00_{\text{H}}$ " upon detection of the specified count start edge of an external input signal. Upon detection of the specified count end edge, the count value is transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) and the interrupt flag (T00CR1/T01CR1:IR) and buffer full flag (T00CR1/T01CR1:BF) are set to "1". The buffer full flag is set to "0" when the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) is read from.

The 8/16-bit compound timer 00/01 data register holds data with the buffer full flag set to "1". Even when the next edge is detected at this time, the next measurement result is lost as the count value is not transferred to the 8/16-bit compound timer 00/01 data register.

As the exception, when the H-pulse and cycle measurement (T00CR0/T01CR0:F3, F2, F1, F0 =  $1001_B$ ) is selected, the H-pulse measurement result is transferred to the 8/16-bit compound timer 00/01 data register with the BF bit set to "1", but the cycle measurement result is not transferred to the 8/16-bit compound timer 00/01 data register with the BF bit set to "1". For cycle measurement, therefore, the H-pulse measurement result must be read before the cycle is completed. Note also that the result of H-pulse measurement or cycle measurement is lost unless read before the completion of the next H pulse.

To measure the time exceeding the length of the counter, you can use software to count the number of occurrences of a counter overflow. When the counter causes an overflow, the interrupt flag (T00CR1/T01CR1:IF) is set to "1". The interrupt service routine can therefore be used to count the number of times the overflow occurs. Note also that an overflow toggles the timer output. The timer output initial value can be set by the timer output initial value bit (T00CR1/T01CR1:SO).

When the timer stops operation, the timer output bit (TMCR0:TO1/TO0) holds the last value.

The value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) must be nullified if an interrupt occurs before the timer is activated (before "1" is written to the STA bit).



Figure 15.12-2 Operating Diagram of PWC Timer (Example of H-pulse Width Measurement)

## 15.13 Operating Description of Input Capture Function

## This section describes the operations of the input capture function for the 8/16-bit compound timer.

### Operation of Input Capture Function

The compound timer requires the settings shown in Figure 15.13-1 to serve as the input capture function.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
T00CR0/T01CR0	IFE	C2	C1	C0	F3	F2	F1	F0
	О	О	О	О	О	О	О	0
T00CR1/T01CR1	STA	HO	IE	IR	BF	IF	SO	OE
	1	О	О	О	×	О	×	×
TMCR	TO1	TO0	IIS	MOD	FE11	FE10	FE01	FE00
	×	×	0	0	О	О	О	О
T00DR/T01DR	R Holds pulse width measurement value							
	O: Used bit							
	x: Unused	bit						
	1: Set "1"							

Figure 15.13-1 Settings for Input Capture Function

When the input capture function is selected, the counter value is stored to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) upon detection of an edge of the external signal input. The edge to be detected is selected by timer operation mode setting (T00CR0/T01CR0:F3, F2, F1, F0).

This function is available in either free-run mode or clear mode, which can be selected by timer operation mode setting.

In clear mode, the counter starts counting from " $00_{\text{H}}$ ". When the edge is detected, the counter value is transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR), the interrupt flag (T00CR1/T01CR1:IR) is set to "1", and the counter continues to count by restarting at " $00_{\text{H}}$ ".

When the edge is detected in free-run mode, the counter value is transferred to the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) and the interrupt flag (T00CR1/T01CR1:IR) is set to "1". In this case, the counter continues to count without being cleared.

This function has no effect on the buffer full flag (T00CR1/T01CR1:BF).

To measure the time exceeding the length of the counter, software can be used to count the number of occurrences of a counter overflow. When the counter causes an overflow, the interrupt flag (T00CR1/T01CR1:IF) is set to "1". The interrupt service routine can therefore be used to count the number of times the overflow occurs.

The capture value in the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) must be nullified if an interrupt occurs before the timer is activated (before "1" is written to the STA bit).





### 15.14 Operating Description of Noise Filter

### This section describes the operations of the noise filter for the 8/16-bit compound timer.

When the input capture or PWC timer function has been selected, a noise filter can be used to eliminate the pulse noise of the signal from the external input pin (EC0/EC1). H-pulse noise, L-pulse noise, or H/L-pulse noise elimination can be selected depending on the register setting (TMCR0:FE11, FE10, FE01, FE00). The maximum pulse width from which to eliminate noise is three machine clock cycles. When the filter function is active, the signal input is subject to a delay of four machine clock cycles.



### 15.15 States in Each Mode during Operation

This section describes how the 8/16-bit compound timer behaves when the microcontroller enters watch mode or stop mode or when a suspend (T00CR1/T01CR1:HO = 1) request is issued during operation.

### ■ When Interval Timer, Input Capture, or PWC Function Has Been Selected

Figure 15.15-1 shows how the counter value changes when transition to watch mode or stop mode or a suspend request occurs during operation of the 8/16-bit compound timer.

The counter stops operation while holding the value when transition to stop mode or watch mode occurs. When the stop mode or watch mode is canceled by an interrupt, the counter resumes operation with the last value held. So the first interval time and external clock count are incorrect. After releasing from stop mode or watch mode, be sure to initialize the counter value.



Figure 15.15-1 Operations of Counter in Standby Mode or in Pause (Not Serving as PWM Timer)



Figure 15.15-2 Operations of Counter in Standby Mode or in Pause (Serving as PWM Timer)

### 15.16 Precautions when Using 8/16-bit Compound Timer

## This section explains the precautions to be taken when using the 8/16-bit compound timer.

### Precautions when Using 8/16-bit Compound Timer

When changing the timer function by using the timer operation mode select bits (T00CR0/T01CR0:F3, F2, F1, F0), the timer operation must be stopped (T00CR1/T01CR1:STA = 0) before clearing the interrupt flag (T00CR1/T01CR1:IF, IR), interrupt enable bits (T00CR1/T01CR1:IE, T00CR0/T01CR0:IFE) and buffer full flag (T00CR1/T01CR1:BF).

When the PWC or input capture function has been selected, an interrupt may occur even before the timer is activated (STA = 0). Therefore, nullify the value of the 8/16-bit compound timer 00/01 data register (T00DR/T01DR) obtained before the activation.

# *CHAPTER 16 8/16-BIT PPG*

This chapter describes the functions and operations of the 8/16-bit PPG.

- 16.1 Overview of 8/16-bit PPG
- 16.2 Configuration of 8/16-bit PPG
- 16.3 Channels of 8/16-bit PPG
- 16.4 Pins of 8/16-bit PPG
- 16.5 Registers of 8/16-bit PPG
- 16.6 Interrupts of 8/16-bit PPG
- 16.7 Operating Description of 8/16-bit PPG
- 16.8 Precautions when Using 8/16-bit PPG
- 16.9 Sample Programs for 8/16-bit PPG Timer

### 16.1 Overview of 8/16-bit PPG

The 8/16-bit PPG is an 8-bit reload timer module that uses pulse output control based on timer operation to perform PPG output. The 8/16-bit PPG also operates in cascade (8 bits + 8 bits) as 16-bit PPG.

### ■ Overview of 8/16-bit PPG

The following section summarizes the 8/16-bit PPG functions.

• 8-bit PPG output independent operation mode

In this mode, the unit can operate as 2 8-bit PPG (PPG timer 00 and PPG timer 01).

• 8-bit prescaler + 8-bit PPG output operation mode

The rising and falling edge detection pulses from the PPG timer 01 output can be inputted to the down-counter of the PPG timer 00 to enable variable-cycle 8-bit PPG output.

16-bit PPG output operation mode

The unit can also operate in cascade (PPG timer 01 (upper 8 bits) + PPG timer 00 (lower 8 bits)) as 16-bit PPG output.

#### PPG output operation

In this operation, a variable-cycle pulse waveform is outputted in any duty ratio.

The unit can also be used as a D/A converter in conjunction with an external circuit.

• Output inversion mode

This mode can invert the PPG output value.

### 16.2 Configuration of 8/16-bit PPG

### This section shows the block diagram of 8/16-bit PPG.

### ■ Block Diagram of 8/16-bit PPG

Figure 16.2-1 shows the block diagram of the 8/16-bit PPG.





#### Counter clock selector

The clock for the countdown of 8-bit down counter is selected from eight types of internal count clocks.

#### 8-bit down-counter

It counts down with the count clock selected with the count clock selector.

#### Comparator circuit

The output is kept "H" until the value of 8-bit down counter is corresponding to the value of 8/16-bit PPG duty setup buffer register from the value of 8/16-bit set buffer register of PPG cycle.

Afterwards, after keep "L" the output until the counter value is corresponding to "1", it keeps counting 8-bit down counter from the value of 8/16-bit PPG cycle setup buffer register.

#### 8/16-bit PPG timer 01 control register (PC01)

The operation condition on the PPG timer 01 side of 8/16-bit PPG timer is set.

8/16-bit PPG timer 00 control register (PC00)

The operation mode of 8/16-bit PPG timer and the operation condition on the PPG timer 00 side are set.

● 8/16-bit PPG timer 01/00 cycle setup buffer register ch.0 (PPS01), 0(PPS00)

The compare value for the cycle of 8/16-bit PPG timer is set.

8/16-bit PPG timer 01/00 duty setup buffer register ch.0 (PDS01), 0(PDS00)

The compare value for "H" width of 8/16-bit PPG timer is set.

8/16-bit PPG start register

The start or the stop of 8/16-bit PPG timer is set.

8/16-bit PPG output inversion register

An initial level also includes the output of 8/16-bit PPG timer and it is reversed.

### Input Clock

The 8/16-bit PPG uses the output clock from the prescaler as its input clock (count clock).

### 16.3 Channels of 8/16-bit PPG

### This section describes the channels of the 8/16-bit PPG.

### Channels of 8/16-bit PPG

MB95130/M series has two channels of the 8/16-bit PPG. There are 8-bit PPG timer 00 and 8-bit PPG timer 01 in 1 channel. They can be used respectively as two 8-bit PPGs. Also, they can be used as a 16-bit PPG.

Table 16.3-1 and Table 16.3-2 show the channels and their corresponding pins and registers.

Table 16.3-1 PINS OF 8/16-DIT P
---------------------------------

Channel	Pin name	Pin function
0	PPG00	PPG timer 00 (8-bit PPG (00), 16-bit PPG)
0	PPG01	PPG timer 01 (8-bit PPG (01), 8-bit prescaler)
1	PPG10	PPG timer 00 (8-bit PPG (10), 16-bit PPG)
1	PPG11	PPG timer 01 (8-bit PPG (11), 8-bit prescaler)

Table 16.3-2 Registers of 8/16-bit PPG

Channel	Register name	Corresponding register (as written in this manual)			
0	PC01	8/16-bit PPG timer 01 control register			
	PC00	8/16-bit PPG timer 00 control register			
	PPS01	8/16-bit PPG timer 01 cycle setup buffer register			
	PPS00	8/16-bit PPG timer 00 cycle setup buffer register			
	PDS01	8/16-bit PPG timer 01 duty setup buffer register			
	PDS00	8/16-bit PPG timer 00 duty setup buffer register			
1	PC11	8/16-bit PPG timer 01 control register			
	PC10	8/16-bit PPG timer 00 control register			
	PPS11	8/16-bit PPG timer 01 cycle setup buffer register			
	PPS10	8/16-bit PPG timer 00 cycle setup buffer register			
	PDS11	8/16-bit PPG timer 01 duty setup buffer register			
	PDS10	8/16-bit PPG timer 00 duty setup buffer register			
Both channels	PPGS	8/16-bit PPG start register			
Both channels	REVC	8/16-bit PPG output inversion register			

The following sections describe only the 8/16-bit PPG in ch.0 side.

### 16.4 Pins of 8/16-bit PPG

This section describes the pins of the 8/16-bit PPG.

### ■ Pins of 8/16-bit PPG

• PPG00 pin and PPG01 pin

These pins function both as general-purpose I/O ports and 8/16-bit PPG outputs.

PPG00, PPG01: A PPG waveform is outputted to these pins. The PPG waveform can be outputted by enabling the output by the 8/16-bit PPG timer 01/00 control registers (PC0: POEN0 = 1, PC1: POEN1 = 1).

### ■ Block Diagram of Pins Related to 8/16-bit PPG



Figure 16.4-1 Block Diagram of Pins (PPG00, PPG01) Related to 8/16-bit PPG

Figure 16.4-2 Block Diagram of Pins (PPG10, PPG11) Related to 8/16-bit PPG



## 16.5 Registers of 8/16-bit PPG

### This section describes the registers of the 8/16-bit PPG.

### ■ Registers of 8/16-bit PPG

Figure 16.5-1 shows the registers of the 8/16-bit PPG.

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
003A <sub>H</sub> PC01	-	-	PIE1	PUF1	POEN1	CKS12	CKS11	CKS10	00000000 <sub>B</sub>
	R0/WX	R0/WX	R/W	R(RM1),W	R/W	R/W	R/W	R/W	
8/16-bit PPG timer	00 contro	l register	(PC00)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
003B <sub>H</sub> PC00	MD1	MD0	PIE0	PUF0	POEN0	CKS02	CKS01	CKS00	00000000 <sub>B</sub>
	R/W	R/W	R/W	R(RM1),W	R/W	R/W	R/W	R/W	
8/16-bit PPG timer	01 cycle	setup buff	er registe	r (PPS01)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0F9C <sub>H</sub> PPS01	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/16-bit PPG timer	00 cycle	setup buff	er registe	r (PPS00)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0F9D <sub>H</sub> PPS00	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/16-bit PPG timer	01 duty s	etup buffe	er register	(PDS01)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0F9E <sub>H</sub> PDS01	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/16-bit PPG timer	00 duty s	etup buffe	er register	(PDS00)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Reset value
0F9F <sub>H</sub> PDS00	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/16-bit PPG start	register (F	PPGS)							
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FA4 <sub>H</sub>	-	-	-	-	PEN11	PEN10	PEN01	PEN00	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/16-bit PPG outpu	ut inversio	n register	(REVC)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FA5 <sub>H</sub>	-	-	-	-	REV11	REV10	REV01	REV00	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
R/W: Rea	dable/writ	able (Rea	d value is	the same	as write v	value)			

### Figure 16.5-1 Registers of 8/16-bit PPG
## 16.5.1 8/16-bit PPG Timer 01 Control Register ch.0 (PC01)

## The 8/16-bit PPG timer 01 control register ch.0 (PC01) sets the operating conditions for PPG timer 01.

#### ■ 8/16-bit PPG Timer 01 Control Register ch.0 (PC01)



#### Figure 16.5-2 8/16-bit PPG Timer 01 Control Register ch.0 (PC01)

	Bit name	Function
bit7 bit6	-: Undefined bits	These bits are undefined. <ul> <li>Writing to the bits is meaningless.</li> <li>Read always returns "0".</li> </ul>
bit5	PIE1: Interrupt request enable bit	This bit controls interrupts of PPG timer 01. <b>Setting the bit to "0"</b> : disables interrupts of PPG timer 01. <b>Setting the bit to "1"</b> : enables interrupts of PPG timer 01. The bit outputs an interrupt request (IRQ) when the counter borrow detection bit (PUF1) and the PIE1 bit are both set to "1".
bit4	PUF1: Counter borrow detection flag bit for PPG cycle down- counter	<ul> <li>This bit serves as the counter borrow detection flag for the PPG cycle down-counter of the PPG timer 01.</li> <li>This bit is set to "1" when a counter borrow occurs during 8-bit PPG mode or 8-bit prescaler mode.</li> <li>In 16-bit PPG mode, this bit is not set to "1" even when a counter borrow occurs.</li> <li>Writing "1" to the bit is meaningless.</li> <li>Writing "0" clears the bit.</li> <li>"1" is read in read-modify-write (RMW) instruction.</li> <li>When the bit is set to "0": a counter borrow is undetected.</li> <li>When the bit is set to "1": a counter borrow is detected.</li> </ul>
bit3	POEN1: Output enable bit	This bit enables or disables the output of PPG timer 01 pin. When the bit is set to "0": the PPG timer 01 pin is used as a general-purpose port. When the bit is set to "1": the PPG timer 01 pin is used as the PPG output pin. Setting this bit to "1" during 16-bit PPG operation mode sets the PPG timer 01 pin as an output. (The setting value of REV01 is outputted. "L" output is supplied when REV01 is 0.)
bit2 bit1 bit0	CKS12, CKS11, CKS10: Operating clock select bits	<ul> <li>These bits select the operating clock for 8-bit down-counter of the PPG timer 01.</li> <li>The operating clock is generated from the prescaler. Refer to "CHAPTER 6 CLOCK CONTROLLER".</li> <li>In 16-bit PPG operation mode, the setting of this bit has no effect on the operation. "000<sub>B</sub>": 1/MCLK</li> <li>"000<sub>B</sub>": 2/MCLK</li> <li>"010<sub>B</sub>": 4/MCLK</li> <li>"011<sub>B</sub>": 8/MCLK</li> <li>"101<sub>B</sub>": 32/MCLK</li> <li>"110<sub>B</sub>": 2<sup>7</sup>/F<sub>CH</sub></li> <li>"111<sub>B</sub>": 2<sup>8</sup>/F<sub>CH</sub></li> <li>Note: Use of a sub clock (in two-system clock product) stops the timebase timer operation. Therefore, selecting "110<sub>B</sub>" or "111<sub>B</sub>" is prohibited.</li> </ul>

Table 16.5-1 8/16-bit PPG Timer 01 Control Register (PC01)

## 16.5.2 8/16-bit PPG Timer 00 Control Register ch.0 (PC00)

The 8/16-bit PPG timer 00 control register ch.0 (PC00) sets the operating conditions and the operation mode for PPG timer 00.

#### ■ 8/16-bit PPG Timer 00 Control Register ch.0 (PC00)



#### Figure 16.5-3 8/16-bit PPG Timer 00 Control Register ch.0 (PC00)

Table 16.5-2 8/16-bit PPG0 Control Register (PC0)

	Bit name	Function
bit7 bit6	MD1, MD0: Operation mode select bits	These bits select the PPG operation mode. Do not modify the bit settings during counting. When set to "00 <sub>B</sub> ": 8-bit PPG independent mode When set to "01 <sub>B</sub> ": 8-bit prescaler + 8-bit PPG mode When set to "1x <sub>B</sub> ": 16-bit PPG mode
bit5	PIE0: Interrupt request enable bit	<ul> <li>This bit controls interrupts of PPG timer 00.</li> <li>Set this bit in 16-bit PPG operation mode.</li> <li>Setting the bit to "0": disables interrupts of PPG timer 00.</li> <li>Setting the bit to "1": enables interrupts of PPG timer 00.</li> <li>An interrupt request (IRQ) is outputted when the counter borrow detection bit (PUF0) and PIE0 bit are both set to "1".</li> </ul>
bit4	PUF0: Counter borrow detection flag bit for PPG cycle down- counter	<ul> <li>This is the counter borrow detection flag for the PPG cycle down-counter of PPG timer 00.</li> <li>Only this bit is effective in 16-bit PPG operation mode (PC1:PUF1 is not operable). Note: Always effective in 8-bit mode</li> <li>Writing "1" to this bit is meaningless.</li> <li>Writing "0" clears the bit.</li> <li>"1" is read in read-modify-write (RMW) instruction.</li> <li>When set to "0": Counter borrow of PPG timer 00 undetected</li> <li>When set to "1": Counter borrow of PPG timer 00 detected</li> </ul>
bit3	POEN0: Output enable bit	<ul> <li>This bit enables or disables the output of PPG timer 00 pin.</li> <li>When set to "0": PPG timer 00 pin is used as a general-purpose port.</li> <li>When set to "1": PPG timer 00 pin is used as the PPG output pin.</li> <li>As the output is supplied from the PPG timer 00 pin in 16-bit PPG operation mode, this bit is used to control the operation.</li> </ul>
bit2 bit1 bit0	CKS02, CKS01, CKS00: Operating clock select bits	<ul> <li>These bits select the operating clock for PPG down-counter PPG timer 00.</li> <li>The operating clock is generated from the prescaler. Refer to "CHAPTER 6 CLOCK CONTROLLER".</li> <li>The rising and falling edge detection pulses from the PPG timer 01 output are used as the count clock for PPG timer 00 when the 8-bit prescaler + 8-bit PPG mode has been selected. Therefore, the setting of this bit has no effect on the operation.</li> <li>Set this bit in 16-bit PPG operation mode.</li> <li>"000<sub>B</sub>": 1/MCLK</li> <li>"001<sub>B</sub>": 2/MCLK</li> <li>"001<sub>B</sub>": 4/MCLK</li> <li>"010<sub>B</sub>": 4/MCLK</li> <li>"101<sub>B</sub>": 32/MCLK</li> <li>"111<sub>B</sub>": 2<sup>8</sup>/F<sub>CH</sub></li> <li>"111<sub>B</sub>": 2<sup>8</sup>/F<sub>CH</sub></li> <li>Note: Use of a sub clock (in two-system clock product) stops the timebase timer operation. Therefore, selecting "110<sub>B</sub>" or "111<sub>B</sub>" is prohibited.</li> </ul>

# 16.5.3 8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register (PPS01/PPS00)

The 8/16-bit PPG timer 00/01 cycle setup buffer register (PPS01/PPS00) sets the PPG output cycle.

#### ■ 8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register (PPS01/PPS00)

PPS01	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	11111111 <sub>B</sub>
0F9C <sub>H</sub> PPS01	R/W								
0FA0 <sub>H</sub> PPS11									
PPS00	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	11111111 <sub>B</sub>
0F9D <sub>H</sub> PPS00	R/W								
OFA1 DDS10									

Figure 16 5-4	8/16-hit PPG	Timor 00/01	Cucla Satur	Buffer Regist	or (DDS01/DDS00)
Figure 10.5-4	0/10-DILFFG		Cycle Selup	J Dullel Regisi	

This register is used to set the PPG output cycle.

- In 16-bit PPG mode, PPS01 serves as the upper 8 bits, while PPS00 serves as the lower 8 bits.
- In 16-bit PPG mode, write the upper bits before the lower bits. When only the upper bits are written, the previously written value is reused in the next load.
- 8-bit mode: Cycle = max. 255 (FF<sub>H</sub>) × Input clock cycle
- 16-bit mode: Cycle = max. 65535 (FFFF<sub>H</sub>) × Input clock cycle
- Initialized at reset.
- Do not set the cycle to  $"00_{\text{H}}"$  or  $"01_{\text{H}}"$  when using the unit in 8-bit PPG independent mode, or in 8-bit prescaler mode + 8-bit PPG mode
- Do not set the cycle to  $"0000_{\text{H}}"$  or  $"0001_{\text{H}}"$  when using the unit in 16-bit PPG mode.
- If the cycle settings are modified during the operation, the modified settings will be effective from the next PPG cycle.

### 16.5.4 8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/ PDS00)

The 8/16-bit PPG timer 00/01 duty setup buffer register (PDS01/PDS00) sets the duty of the PPG output.

#### ■ 8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/PDS00)

PDS01	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0	11111111 <sub>B</sub>
0F9E <sub>H</sub> PDS01	R/W								
0FA2 <sub>H</sub> PDS11									
PDS00	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	11111111 <sub>B</sub>
0F9F <sub>H</sub> PDS00	R/W								
0FA3⊔ PDS10									

#### Figure 16.5-5 8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/PDS00)

This register is used to set the duty of the PPG output ("H" pulse width when normal polarity).

- In 16-bit PPG mode, PDS01 serves as the upper 8 bits while PDS00 serves as the lower 8 bits.
- In 16-bit PPG mode, write the upper bits before the lower bits. When only the upper bits are written, the previously written value is reused in the next load. By writing to PDS00, PDS01 is updated.
- Initialized at reset.
- To set the duty to 0%, select " $00_{\text{H}}$ ".
- To set the duty to 100%, set it to the same value as the 8/16-bit PPG timer 00/01 cycle setup register (PPS00, 01).
- When the 8/16-bit PPG timer 00/01 duty setup register (PDS) is set to a larger value than the setting value of the 8/16-bit PPG cycle setup buffer register (PPS), the PPG output becomes "L" output in the normal polarity (when the output level inversion bit of 8/16-bit PPG output inversion register is "0").
- If the duty settings are modified during operation, the modified value will be effective from the next PPG cycle.

## 16.5.5 8/16-bit PPG Start Register (PPGS)

The 8/16-bit PPG start register (PPGS) starts or stops the down-counter. The operation enable bit of each channel is assigned to the PPGS register, allowing simultaneous activation of the PPG channels.

#### ■ 8/16-bit PPG Start Register (PPGS)

A detro o o	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
оFA4н	- *	- *	- *	- *	PEN11	PEN10	PEN01	PEN00	0000000в
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
				<u>-</u>					
				PEN00	PPG tir	ner 00 (c	h.0) dow	vn-counte	r operation enable bit
				0			Stops	operation	<u>n</u>
				1			Enabl	es operat	ion
				PEN01	PPG tir	ner 01 (c	h 0) dow	n-counte	r operation enable bit
				0			Stops	operation	n
				1			Enabl	es operat	ion
				PEN10	PPG tir	ner 00 (c	h.1) dov	vn-counte	r operation enable bit
				0			Stops	operation	n
				1			Enabl	es operat	ion
						nor 01 (c	h 1) dou		r operation anable bit
					FFG III		Stope		
				1			Enabl	es operation	ion
					1		LIIdol	co operat	
R/	W : Read	lable/wr I value	itable (R	ead val	ue is the	same a	s write v	alue)	
*	: Writi	ng to bit	7 to bit4	is mear	ningless.				

Figure 16.5-6 8/16-bit PPG Start Register (PPGS)

## 16.5.6 8/16-bit PPG Output Inversion Register (REVC)

The 8/16-bit PPG output inversion register (REVC) inverts the PPG output including the initial level.

#### ■ 8/16-bit PPG Output Inversion Register (REVC)





### 16.6 Interrupts of 8/16-bit PPG

#### The 8/16-bit PPG outputs an interrupt request when a counter borrow is detected.

#### ■ Interrupts of 8/16-bit PPG

Table 16.6-1 shows the interrupt control bits and interrupt sources of the 8/16-bit PPG.

#### Table 16.6-1 Interrupt Control Bits and Interrupt Sources of 8/16-bit PPG

	Descriptior	l
Item	PPG timer 01 (8-bit PPG, 8-bit prescaler)	PPG timer 00 (8-bit PPG, 16-bit PPG)
Interrupt request flag bit	PUF1 bit in PC1	PUF0 bit in PC0
Interrupt request enable bit	PIE1 bit in PC1	PIE0 bit in PC0
Interrupt source	Counter borrow of PPG cyc	le down-counter

When a counter borrow occurs on the down-counter, the 8/16-bit PPG sets the counter borrow detection flag bit (PUF) in the 8/16-bit PPG timer 00/01 control register (PC) to "1". When the interrupt request enable bit is enabled (PIE = 1), an interrupt request is outputted to the interrupt controller.

In 16-bit PPG mode, the 8/16-bit PPG timer 00 control register (PC00) is available.

#### ■ Registers and Vector Table Related to Interrupts of 8/16-bit PPG

Interrupt	Interrupt	Interrupt level	setup register	Vector table address		
source	source request No.		Setting bit	Upper	Lower	
ch.0 (upper)	IRQ12	ILR3	L12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	
ch.0 (lower)	IRQ13	ILR3	L13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	

#### Table 16.6-2 Registers and Vector Table Related to Interrupts of 8/16-bit PPG

ch. : channel

Refer to "APPENDIX B Table of Interrupt Causes" for the interrupt request numbers and vector tables of all peripheral functions.

## 16.7 Operating Description of 8/16-bit PPG

#### This section describes the operations of the 8/16-bit PPG.

#### Setup Procedure Example

The setup procedure of the 8/16-bit PPG is described below.

#### Initial setup

- 1) Set the port output (DDR2, DDR6)
- 2) Set the interrupt revel (ILR2, ILR3)
- 3) Select the operating clock, enable the output and interrupt (PC01)
- 4) Select the operating clock, enable the output and interrupt, select the operation mode (PC00)
- 5) Set the cycle (PPS)
- 6) Set the duty (PDS)
- 7) Set the output inversion (REVC)
- 8) Start PPG (PPGs)

Interrupt processing

- 1) Process any interrupt
- 2) Clear the interrupt request flag (PC01: PUF1, PC00: PUF0)
- 3) Start PPG (PPGS)

## 16.7.1 8-bit PPG Independent Mode

## In this mode, the unit operates as two channels (PPG timer 00 and PPG timer 01) of the 8-bit PPG.

#### Setting 8-bit Independent Mode

The unit requires the register settings shown in Figure 16.7-1 to operate in 8-bit independent mode.

		<u> </u>							
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
PC01	-	-	PIE1	PUF1	POEN1	CKS12	CKS11	CKS10	
			0	0	0	0	0	0	
PC00	MD1	MD0	PIE0	PUF0	POEN0	CKS02	CKS01	CKS00	
	0	0	0	0	0	0	0	$\odot$	
		DUC	DUC			DUO	DU4	DUO	
PP501		PHO		PH4			PHI	PHU	
		Se	et PPG 0	utput cy	cie for PH	G timer	01		
PP500		PL6		PL4		PL2	PL1	PLU	
		SE	IPPG 0	uipui cy		-G limer	00 —		
PD901		рне							
FD301					ty for DD	C timor (			
		3e		ութու ու		Gumer	JI —		
PDS00	DH7	DH6	DH5		DH3	DH2	DH1		
1 0000					ity for PP	G timer (	10 <u> </u>		
		00		uipui ui		O unier v	50		
PPGS	-	-	-	-	PEN11	PEN10	PEN01	PEN00	
	*	*	*	*	*	*	@	<u> </u>	
							Ŭ	0	
REVC	-	-	-	-	REV11	REV10	REV01	REV00	
	*	*	*	*	*	*	0	<u> </u>	
⊚ : Used	l bit								
0 : Set "	0"								
* : The	bit status	depends	on the r	number o	of channe	els provid	ded.		

Figure 16.7-1 8-bit Independent Mode

#### Operation of 8-bit PPG Independent Mode

- This mode is selected when the operation mode select bits (MD1, 0) in the 8/16-bit PPG timer 00 control register (PC00) are set to "00<sub>B</sub>".
- When the corresponding bit (PEN) in the 8/16-bit PPG start register (PPGS) is set to "1", the value in the 8/16-bit PPG cycle setup buffer register (PPS) is loaded to start down-count operation. When the count value reaches "1", the value in the cycle setup register is reloaded to repeat the counting.
- "H" is output to the PPG output synchronizing with the count clock. When the down-counter value matches the value in the 8/16-bit PPG timer 00/01 duty setup buffer register (PDS). After "H" which is the value of duty setting is output, "L" is output to the PPG output.

If, however, the PPG output inversion bit is set to "1", the PPG output is set and reset inversely from the above process.

Figure 16.7-2 shows the operation of the 8-bit PPG independent mode.



Figure 16.7-2 Operation of 8-bit PPG Independent Mode

Example for setting the duty to 50%

When PDS is set to " $02_{\text{H}}$ " with PPS set to " $04_{\text{H}}$ ", the PPG output is set at a duty ratio of 50% (PPS setting value /2 set to PDS).

## 16.7.2 8-bit Prescaler + 8-bit PPG Mode

In this mode, the rising and falling edge detection pulses from the PPG timer 01 output can be used as the count clock of the PPG timer 00 down-counter to allow variable-cycle 8-bit PPG output from PPG timer 00.

#### Setting 8-bit Prescaler + 8-bit PPG Mode

The unit requires the register settings shown in Figure 16.7-3 to operate in 8-bit prescaler + 8-bit PPG mode.



#### Figure 16.7-3 Setting 8-bit Prescaler + 8-bit PPG Mode

#### Operation of 8-bit Prescaler + 8-bit PPG Mode

- This mode is selected by setting the operation mode select bits (MD1, 0) of the 8/16-bit PPG timer 00 control register (PC00) to "01<sub>B</sub>". This allows PPG timer 01 to be used as an 8-bit prescaler and PPG timer 00 to be used as an 8-bit PPG.
- When the PPG timer 00 (ch.1) down counter operation enable bit (PEN01) is set to "1", the 8-bit prescaler (PPG timer 01) loads the value in the 8/16-bit PPG timer 01 cycle setup buffer register (PPS01) and starts down-count operation. When the value of the down-counter matches the value in the 8/16-bit PPG timer 01 duty setup buffer register (PDS01), the PPG01 output is set to "H" synchronizing with the count clock. After "H" which is the value of duty setting is output, the PPG01 output is set to "L". If the output inversion signal (REV01) is "0", the polarity will remain the same. If it is "1", the

polarity will be inverted and the signal will be outputted to the PPG pin.

- When the PPG operation enable bit (PEN00) is set to "1", the 8-bit PPG (PPG timer 00) loads the value in the 8/16-bit PPG timer 00 cycle setup buffer register (PPS00) and starts down-count operation (count clock = rising and falling edge detection pulses of PPG01 output after PPG timer 01 operation is enabled). When the count value reaches "1", the value in the 8/16-bit PPG timer 00 cycle setup buffer register is reloaded to repeat the counting. When the value of the down-counter matches the value in the 8/16-bit PPG timer 00 duty setup buffer register (PDS00), the PPG00 output is set to "H" synchronizing with the count clock. After "H" which is the value of duty setting is output, the PPG00 output is reset to "L". If the output inversion signal (REV00) is "0", the polarity will remain the same. If it is "1", the polarity will be inverted and the signal will be outputted to the PPG00 pin.
- Set that the duty of the 8-bit prescaler (PPG timer 01) output to 50%.
- When PPG timer 00 is started with the 8-bit prescaler (PPG timer 01) being stopped, PPG timer 00 does not count.
- When the duty of the 8-bit prescaler (PPG timer 01) is set to 0% or 100%, PPG timer 00 does not perform counting as the 8-bit prescaler (PPG timer 01) output does not toggle.

Figure 16.7-4 shows the operation of 8-bit prescaler + 8-bit PPG mode.



#### Figure 16.7-4 Operation of 8-bit Prescaler + 8-bit PPG Mode

## 16.7.3 16-bit PPG Mode

## In this mode, the unit can operate as a 16-bit PPG when PPG timer 01 and PPG timer 00 are assigned to the upper and lower bits respectively.

#### ■ Setting 16-bit PPG Mode

The unit requires the register settings shown in Figure 16.7-5 to operate in 16-bit PPG mode.

				J				
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PC01	-	-	PIE1	PUF1	POEN1	CKS12	CKS11	CKS10
			٢	۲	٢	0	0	0
PC00	MD1	MD0	PIE0	PUF0	POEN0	CKS02	CKS01	CKS00
	0	0/1	0	0	0	0	0	0
PPS01	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
	$ \leq $	Set PPG	output c	vcle (Up	per 8 bits	s) for PP	G timer (	01
				) (-F		-,		
PPS00	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0
	<u> </u>	Set PPG	output cy	ycle (Lov	ver 8 bits	) for PPG	6 timer 0	0
PDS01	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0
	<u> </u>	Set PPG	output d	uty (Upp	er 8 bits)	for PPG	timer 07	1
PDS00	DH7	DH6	DH5	DH4	DH3	DH2	DH1	DH0
		Set PPG	output d	uty (Low	er 8 bits	) for PPG	timer 0	0
PPGS	-	-	-	-	PEN11	PEN10	PEN01	PEN00
	*	*	*	*	*	*	×	0
REVC	-	-	-	-	REV11	REV10	REV01	REV00
	*	*	*	*	*	*	×	0
ം : Use	d bit							
0 : Set	"0"							
1 : Set	- "1"							
x Sett	ina nullifie	h						
* · Tho	hit statue	chandee	denendi	na on the	number	of channe	els imple	mented
. 1110	Sit Status	onanges	acpenui	ig on the				menteu.

Figure 16.7-5 Setting 16-bit PPG Mode

#### Operation of 16-bit PPG Mode

- This mode is selected by setting the operation mode select bits (MD1, 0) of the PPG timer 00 control register (PC00) to "10<sub>B</sub>" or "11<sub>B</sub>".
- When the PPG operation enable bit (PEN00) is set to "1" in 16-bit PPG mode, the 8-bit down-counters (PPG timer 00) and 8-bit down-counter (PPG timer 01) load the values in the 8/16-bit PPG timer 00/01 cycle setup buffer registers (PPS01 for PPG timer 01 and PPS00 for PPG timer 00) and start down-count operation. When the count value reaches "1", the values in the cycle setup register are reloaded and the counters repeat the counting.
- When the values of the down-counters match the values in the 8/16-bit PPG timer duty setup buffer registers (both the value in PDS01 for PPG timer 01 and the value in PDS00 for PPG timer 00), the PPG00 pin is set to "H" synchronizing with the count clock. After "H" which is the value of duty setting is output, the PPG00 pin is set to "L". If the output inversion signal (REV00) is "0", the signal will be outputted to the PPG00 with the polarity unchanged. If it is set to "1", the polarity will be inverted and the signal will be outputted to the PPG00 pin. (ch.0 only. ch.1 will be set to the initial value <"L" if REV01 is "0", or "H" if it is "1">>.)

Figure 16.7-6 shows the operation of 16-bit PPG mode.



Figure 16.7-6 Operation of 16-bit PPG Mode

## 16.8 Precautions when Using 8/16-bit PPG

#### The following precautions must be followed when using the 8/16-bit PPG.

#### ■ Precautions when Using 8/16-bit PPG

Operational precaution

Depending on the timing between the activation of PPG and count clock, an error may occur in the first cycle of the PPG output immediately after the activation. The error varies depending on the count clock selected. The output, however, is performed properly in the succeeding cycles.

• Precaution regarding interrupts

A PPG interrupt is generated when the interrupt enable bit (PIE1/PIE0) is set to "1" and the interrupt request flag bit (PUF1/PUF0) in the 8/16-bit PPG timer 01/00 control register (PC01/PC00) is also set to "1". Always clear the interrupt request flag bit (PUF1/PUF0) to "0" in the interrupt routine.

## 16.9 Sample Programs for 8/16-bit PPG Timer

#### We provide sample programs that can be used to operate the 8/16-bit PPG timer.

#### ■ Sample Programs for 8/16-bit PPG Timer

For information about the sample programs for the 8/16-bit PPG timer, refer to "Sample Programs" in Preface.

#### Setup Methods without Sample Program

How to enable/stop PPG operation

The PPG operation enable bit (PPGS:PEN00 or PEN01) is used for PPG00.

Control	PPG operation enable bit (PEN00 or PEN01)
When stopping PPG operation	Set the bit to "0"
When enabling PPG operation	Set the bit to "1"

PPG operation must be enabled before the PPG is activated.

The PPG operation enable bit (PPGS:PEN00 or PEN01) is used for PPG01.

Control	PPG operation enable bit (PEN00 or PEN01)
When stopping PPG operation	Set the bit to "0"
When enabling PPG operation	Set the bit to "1"

PPG operation must be enabled before the PPG is activated.

#### • How to set the PPG operation mode

The operation mode select bits (PC0:MD[1:0]) are used.

#### How to select the operating clock

ch.1 is selected by the operating clock select bits (PC1:CKS12/CKS11/CKS10).

ch.0 is selected by the operating clock select bits (PC0:CKS02/CKS01/CKS00).

#### How to enable/disable the PPG output pin

The output enable bit (PC0 or PC1:POEN0 or POEN1) is used.

Control	Output enable bit (POEN0 or POEN1)
When enabling PPG output	Set the bit to "1"
When disabling PPG output	Set the bit to "0"

• How to invert the PPG output

The output level inversion bit (REVC:REV00 or REV10) is used for PPG00.

Control	Output level inversion bit (REV00 or REV10)
When inverting PPG output	Set the bit to "1"

The output level inversion bit (REVC:REV01 or REV11) is used for PPG01.

Control	Output level inversion bit (REV01 or REV11)
When inverting PPG output	Set the bit to "1"

#### Interrupt-related register

The interrupt level is set by the interrupt setup register shown in the following table.

Interrupt source	Interrupt level setup register	Interrupt vector
ch.1 (lower)	Interrupt level register (ILR2) Address:0007B <sub>H</sub>	#09 Address:0FFE8 <sub>H</sub>
ch.1 (upper)	Interrupt level register (ILR2) Address:0007B <sub>H</sub>	#10 Address:0FFE6 <sub>H</sub>
ch.0 (lower)	Interrupt level register (ILR3) Address:0007C <sub>H</sub>	#12 Address:0FFE2 <sub>H</sub>
ch.0 (upper)	Interrupt level register (ILR3) Address:0007C <sub>H</sub>	#13 Address:0FFE0 <sub>H</sub>

#### How to enable/disable/clear interrupts

Interrupt request enable flag, Interrupt request flag

The interrupt request enable bit (PC00:PIE0 or PC01:PIE1) is used to enable or disable interrupts.

What to be controlled	Interrupt request enable bit (PIE0 or PIE1)
When disabling interrupt requests	Set the bit to "0"
When enabling interrupt requests	Set the bit to "1"

The interrupt request flag (PC00:PUF0 or PC01:PUF1) is used to clear interrupt requests.

What to be controlled	Interrupt request flag (PUF0 or PUF1)
When clearing interrupt requests	Write "0"

#### CHAPTER 16 8/16-BIT PPG

# CHAPTER 17 16-BIT PPG TIMER

This chapter describes the functions and operations of the 16-bit PPG timer.

- 17.1 Overview of 16-bit PPG Timer
- 17.2 Configuration of 16-bit PPG Timer
- 17.3 Channels of 16-bit PPG Timer
- 17.4 Pins of 16-bit PPG Timer
- 17.5 Registers of 16-bit PPG Timer
- 17.6 Interrupts of 16-bit PPG Timer
- 17.7 Explanation of 16-bit PPG Timer Operations and Setup Procedure Example
- 17.8 Precautions when Using 16-bit PPG Timer
- 17.9 Sample Programs for 16-bit PPG Timer

## 17.1 Overview of 16-bit PPG Timer

The 16-bit PPG timer can generate a PWM (Pulse Width Modulation) output or one-shot (square wave) output, and the period and duty of the output waveform can be changed by software freely. The timer can also generate an interrupt when a start trigger occurs or on the rising or falling edge of the output waveform.

#### 16-bit PPG Timer

16-bit PPG timer can output the PWM output and the one shot. The output wave form can be reversed by setting the register (Normal polarity  $\leftrightarrow$  Inverted polarity).



- The count operation clock can be selected from eight different clock sources (MCLK/1, MCLK/2, MCLK/4, MCLK/8, MCLK/16, MCLK/32, F<sub>CH</sub>/2<sup>7</sup>, or F<sub>CH</sub>/2<sup>8</sup>). (MCLK: Machine clock, F<sub>CH</sub>: Clock)
- Interrupt can be selectively triggered by the following four conditions:
  - Occurrence of a start trigger in the PPG timer
  - Occurrence of a counter borrow in the 16-bit down-counter (cycle match).
  - Rising edge of PPG in normal polarity or falling edge of PPG in inverted polarity
  - Counter borrow, rising edge of PPG in normal polarity, or falling edge of PPG in inverted polarity

## 17.2 Configuration of 16-bit PPG Timer

Shown below is the block diagram of the 16-bit PPG timer.

#### Block Diagram of 16-bit PPG Timer



#### Figure 17.2-1 Block Diagram of 16-bit PPG Timer

#### Count clock selector

The clock for the countdown of 16-bit down-counter is selected from eight types of internal count clocks.

#### • 16 bit down-counter

It counts down with the count clock selected with the count clock selector.

#### • Comparator circuit

The output is kept "H" until the value of 16-bit down-counter is corresponding to the value of 8/16-bit PPG duty setting buffer register from the value of 16-bit PPG cycle setting buffer register.

Afterwards, after keep "L" the output until the counter value is corresponding to "1", it keeps counting 8-bit down counter from the value of 16-bit PPG cycle setting buffer register.

16-bit PPG down-counter register (PDCRH, PDCRL)

The value of 16-bit down-counter of 16-bit PPG timer is read.

• 16-bit PPG cycle setting buffer register (PCSRH, PCSRL)

The compare value for the cycle of 16-bit PPG timer is set.

• 16-bit PPG duty setting buffer register (PDUTH, PDUTL)

The compare value for "H" width of 16-bit PPG timer is set.

• 16-bit PPG status control register (PCNTH, PCNTL)

The operation mode and the operation condition of 16-bit PPG timer are set.

#### Input Clock

The 16-bit PPG timer uses the output clock from the prescaler as its input clock (count clock).

## 17.3 Channels of 16-bit PPG Timer

#### This section describes the channels of the 16-bit PPG timer.

#### ■ Channels of 16-bit PPG Timer

MB95130/M series has one16-bit PPG timer.

Table 17.3-1 and Table 17.3-2 show the correspondence among the channel, pin and register.

#### Table 17.3-1 Pins of 16-bit PPG Timer

Channel	Pin name	Pin function
0	PPG0	PPG0 output
0	TRG0	Trigger 0 input

#### Table 17.3-2 Registers of 16-bit PPG Timer

Channel	Register name	Corresponding register (name in this manual)
	PDCRH0	16-bit PPG down counter register (upper)
	PDCRL0	16-bit PPG down counter register (lower)
	PCSRH0	16-bit PPG cycle setting buffer register (upper)
0	PCSRL0	16-bit PPG cycle setting buffer register (lower)
0	PDUTH0	16-bit PPG duty setting buffer register (upper)
	PDUTL0	16-bit PPG duty setting buffer register (lower)
	PCNTH0	16-bit PPG status control register (upper)
	PCNTL0	16-bit PPG status control register (lower)

### 17.4 Pins of 16-bit PPG Timer

#### This section describes the pins of the 16-bit PPG timer.

#### Pins of 16-bit PPG Timer

The pin related to the 16-bit PPG timer is namely the PPG0 pin.

PPG0 pin

Each pin serves as a general-purpose I/O port as well as a 16-bit PPG timer output.

PPG0: A PPG waveform is outputted to these pins. The PPG waveform can be outputted by using the 16bit PPG status control register to enable output (PCNTL0: POEN=1).

• TRG0 pin

TRG0:Used to start 16-bit PPG timer by hardware trigger.

#### Block Diagrams of Pins Related to 16-bit PPG





## 17.5 Registers of 16-bit PPG Timer

#### This section describes the registers of the 16-bit PPG timer.

#### ■ Registers of 16-bit PPG Timer

	Fi	gure 1	7.5-1 F	Register	's of 16	-bit PPC	g Timer	•	
16-bit PPG down o	counter reg	gister (u	pper): Pl	DCRH					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAA <sub>H</sub> PDCRH0	DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08	00000000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	
16-bit PPG down o	counter reg	gister (lo	wer): PI	DCRL					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAB <sub>H</sub> PDCRL0	DC07	DC06	DC05	DC04	DC03	DC02	DC01	DC00	00000000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	
16-bit PPG cycle s	etting buff	er regist	ter (uppe	er): PCSI	RH				
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0FAC <sub>H</sub> PCSRH0	CS15	CS14	CS13	CS12	CS11	CS10	CS09	CS08	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	_
16-bit PPG cycle s	etting buff	er regist	ter (lowe	r): PCSF	RL				
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAD <sub>H</sub> PCSRL0	CS07	CS06	CS05	CS04	CS03	CS02	CS01	CS00	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	D
16-bit PPG duty se	etting buffe	er registe	er (uppe	r): PDUT	Ή				
Address	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0FAE <sub>H</sub> PDUTH0	DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	D
16-bit PPG duty se	etting buffe	er registe	er (lower	): PDUTI	L				
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAF <sub>H</sub> PDUTL0	DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU01	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	b
16-bit PPG status	control re	gister (u	pper): P	CNTH					
Address	15	14	13	12	11	10	9	8	Initial value
0042 <sub>H</sub> PCNTH0	CNTE	STRG	MDSE	RTRG	CKS2	CKS1	CKS0	PGMS	00000000 <sub>B</sub>
	R/W	R0/W	R/W	R/W	R/W	R/W	R/W	R/W	D
16-bit PPG status	control reg	gister (lo	wer): PC	ONTL					
Address	7	6	5	4	3	2	1	0	Initial value
0043 <sub>H</sub> PCNTL0	EGS1	EGS0	IREN	IRQF	IRS1	IRS0	POEN	OSEL	0000000 <sub>R</sub>
	R/W	R/W	R/W	R(RM1),W	R/W	R/W	R/W	R/W	b
R/W: Rea R/WX: Rea	dable/writ d only (Re	able (Re adable,	ad value writing h	e is the s nas no ef	ame as fect on c	write valu	) )		
R(RM1), W: Rea	dable/writ	able (Re	ad value	e is differ	ent from	write val	lue, "1" is	s read by	read-modify-
write	e (RIVIVV) II	nstructio	n)						

## 17.5.1 16- bit PPG Down Counter Registers (PDCRH0, PDCRL0)

The 16-bit PPG down counter registers (PDCRH0, PDCRL0) form a 16-bit register which is used to read the count value from the 16-bit PPG down-counter.

Figure 17.5-2 16-bit PPG Down Counter Registers (PDCRH0, PDCRL0)

#### ■ 16-bit PPG Down Counter Registers (PDCRH0, PDCRL0)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAA <sub>H</sub> PDCRH0	DC15	DC14	DC13	DC12	DC11	DC10	DC09	DC08	00000000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	
16-bit PPG down co	ounter reg	gister (lov	wer) PD(	CRL0	hit?	hit?	hit1	hitO	Initial value
16-bit PPG down co Address	bit7	gister (lov bit6	wer) PD0 bit5	CRL0 bit4	bit3	bit2	bit1	bit0	Initial value
16-bit PPG down co Address 0FAB <sub>H</sub> PDCRL0	bunter reg bit7 DC07	gister (lov bit6 DC06	wer) PD0 bit5 DC05	CRL0 bit4 DC04	bit3 DC03	bit2 DC02	bit1 DC01	bit0 DC00	Initial value 00000000 <sub>B</sub>
16-bit PPG down co Address 0FAB <sub>H</sub> PDCRL0	bit7 bit7 DC07 R/WX	gister (lov bit6 DC06 R/WX	wer) PD0 bit5 DC05 R/WX	CRL0 bit4 DC04 R/WX	bit3 DC03 R/WX	bit2 DC02 R/WX	bit1 DC01 R/WX	bit0 DC00 R/WX	Initial value 00000000 <sub>B</sub>

These registers form a 16-bit register which is used to read the count value from the 16-bit down-counter. The initial values of the register are all "0".

Always use one of the following procedures to read from this register.

- Use the "MOVW" instruction (use a 16-bit access instruction to read the PDCRH0 register address)
- Use the "MOV" instruction and read PDCRH0 first and PDCRL0 second (reading PDCRH0 automatically copies the lower 8 bits of the down-counter to PDCRL0)

These registers are read-only and writing has no effect on the operation.

Note:

If you use the "MOV" instruction and read PDCRL0 before PDCRH0, PDCRL0 will return the value from the previous valid read operation. Therefore, the value of the 16-bit down-counter will not be read correctly.

# 17.5.2 16-bit PPG Cycle Setting Buffer Registers (PCSRH0, PCSRL0)

The 16-bit PPG cycle setting buffer registers are used to set the cycle for the output pulses generated by the PPG.

#### ■ 16-bit PPG Cycle Setting Buffer Registers (PCSRH0, PCSRL0)

1111 <sub>B</sub>
i value
1111⊳
D
1

#### Figure 17.5-3 16-bit PPG Cycle Setting Buffer Registers (PCSRH0, PCSRL0)

These registers form a 16-bit register which sets the period for the output pulses generated by the PPG. The values set in these registers are loaded to the down-counter.

When writing to these registers, always use one of the following procedures.

- Use the "MOVW" instruction (use a 16-bit access instruction to write to the PCSRH0 register address)
- Use the "MOV" instruction and write to PCSRH0 first and PCSRL0 second If a down-counter load occurs after writing data to PCSRH0 (but before writing data to PCSRL0), the previous valid PCSRH0/PCSRL0 value will be loaded to the down-counter. If the PCSRH0/PCSRL0 value is modified during counting, the modified value will become effective from the next load of the down-counter.
- Do not set PCSRH0 and PCSRL0 to  $"00_{\text{H}}"$ , or PCSRH0 to  $"00_{\text{H}}"$  and PCSRL0 to  $"01_{\text{H}}"$ .

Note:

If the down-counter load occurs after the "MOV" instruction is used to write data to PCSRL0 before PCSRH0, the previous valid PCSRH0 value and newly written PCSRL0 value are loaded to the down-counter. It should be noted that as a result, the correct period cannot be set.

## 17.5.3 16-bit PPG Duty Setting Buffer Registers (PDUTH0, PDUTL0)

The 16-bit PPG duty setting buffer registers control the duty ratio for the output pulses generated by the PPG.

#### ■ 16-bit PPG Duty Setting Buffer Registers (PDUTH0, PDUTL0)

duress	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
0FAE <sub>H</sub> PDUTH0	DU15	DU14	DU13	DU12	DU11	DU10	DU09	DU08	11111111 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ddress	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
ddress	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FAF <sub>H</sub> PDUTL0	DU07	DU06	DU05	DU04	DU03	DU02	DU01	DU01	11111111 <sub>B</sub>
		R/\//	R/W	R/W	R/W	R/W	R/W	R/W	

#### Figure 17.5-4 16-bit PPG Duty Setting Buffer Registers (PDUTH0, PDUTL0)

These registers form a 16-bit register which controls the duty ratio for the output pulses generated by the PPG. Transfer of the data from the 16-bit PPG duty setting buffer registers to the duty setting registers is performed at the same timing as the down-counter read.

When writing to these registers, always use one of the following procedures.

- Use the "MOVW" instruction (use a 16-bit access instruction to write to the PDUTH0 register address)
- Use the "MOV" instruction and write to PDUTH0 first and PDUTL0 second If a down-counter load occurs after writing data to PDUTH0 (but before writing data to PDUTL0), the value of the 16-bit PPG duty setting buffer registers is not transferred to the duty setting registers.

The relation between the value of the 16-bit PPG duty setting registers and output pulse is as follows:

- When the same value is set in both the 16-bit PPG cycle setting buffer registers and duty setting registers, the "H" level will always be outputted if normal polarity is set, or the "L" level will always be outputted if inverted polarity is set.
- When the duty setting registers are set to "00<sub>B</sub>", the "L" level will always be outputted if normal polarity is set, or the "H" level will always be outputted if inverted polarity is set.
- When the value set in the duty setting registers is greater than the value in the 16-bit PPG cycle setting buffer registers, the "L" level will always be outputted if normal polarity is set, and the "H" level will always be outputted if inverted polarity is set.

## 17.5.4 16-bit PPG Status Control Register (PCNTH0, PCNTL0)

The 16-bit PPG status control register is used to enable and disable the 16-bit PPG timer and also to set the operating status for the software trigger, retrigger control interrupt, and output polarity. This register can also check the operation status.

#### ■ 16-bit PPG Status Control Register, Upper Byte (PCNTH0)



Figure 17.5-5 16-bit PPG Status Control Register, Upper Byte (PCNTH0)

Bit name		Function					
bit7	CNTE: Timer enable bit	This bit is used to enable/stop PPG timer operation. <b>When the bit is set to ''0''</b> , the PPG operation halts immediately and the PPG output goes to the initial level ("L" output if OSEL is 0; "H" output if OSEL is 1). <b>When the bit is set to ''1''</b> , PPG operation is enabled and the PPG goes to standby to wait for a trigger.					
bit6	STRG: Software trigger bit	This bit is used to start the PPG timer by software. When the bit is set to "1", setting the CNTE bit to "1" starts the PPG timer. Reading this bit always returns "0".					
bit5	MDSE: Mode select bit	This bit is used to set the PPG operation mode.         When the bit is set to "0", the PPG operates in PWM mode.         When the bit is set to "1", the PPG operates in one-shot mode.         Note:       Modifying this bit is prohibited during operation.					
bit4	RTRG: Software retrigger enable bit	This bit is used to enable or disable the software retrigger function of the PPG during operation. When the bit is set to "0", the software retrigger function is "disabled". When the bit is set to "1", the software retrigger function is "enabled".					
bit1 bit2 bit3	CKS2~CKS0: Count clock select bits	<ul> <li>These bits select the operating clock for the 16-bit PPG timer.</li> <li>The count clock signal is generated by the prescaler. Refer to "6.12 Operating Explanation of Prescaler".</li> <li>Note: As the timebase timer (TBT) is halted in sub clock mode, F<sub>CH</sub>/2<sup>7</sup> and F<sub>CH</sub>/2<sup>8</sup> cannot be selected in this case.</li> </ul>					
bit0	PGMS: PPG output mask enable bit	This bit is used to mask the PPG output to a specific level regardless of the mode setting (MDSE: bit5), period setting (PCSRH0, PCSRL0), and duty setting (PDUTH0, PDUTL0). When the bit is set to "0", the PPG output mask function is disabled. When the bit is set to "1", the PPG output mask function is enabled. When the PPG output polarity setting is set to "normal" (OSEL bit in PCNTL0 register = 0), the output is always masked to "L". When the polarity setting is set to "inverted" (OSEL bit in PCNTL0 register = 1), the PPG output is always masked to "H".					

Table 17.5-1 16-bit PPG Status Control Register, Upper Byte (PCNTH0)

### ■ 16-bit PPG Status Control Register, Lower Byte (PCNTL0)

Address	bit7 EGS1	bit6 EGS0	bit5 IREN	bit4	bit3	bit2	bit1	bit0	Initial value 00000000 <sub>B</sub>	
	R/W	R/W	R/W	R(RM1),	W R/W	/ R/W	R/W	/ R/W	 '	
							OSEL		Output inversio	n bit
							0		Normal polar	ity
							1		Inverted pola	rity
						<b> </b>	POEN		Output enable	e bit
							0		General-purpose	I/O port
							1		PPG output p	bin
						<b>↓</b>	RS1	IRS0	Interrupt type	e select bit
							0	0	Trigger, software tr retrigger by TRG ir	igger, and nput
							0	1	Counter borrow	
							1	0	Rising edge of PPG polarity or falling edg in inverted polarity (E	output in normal e of PPG output Duty match)
							1	1	Counter borrow, risin output in normal pola edge of PPG output	g edge of PPG irity, or falling in inverted polarity
									PPG interrupt fla	ag bit
							IRQF -		Read	Write
							0	No I	PPG interrupt	Clears this bit
							1	PPG int	terrupt generated	No effect on operation
							IREN	PP	G interrupt request	enable flag
							0		Disables interrupt	request
							1		Enables interrupt	request
						EGS0	ŀ	Hardwar	e trigger enable bit	0
						0	The fal	ling edg	e of TRG has no ef	fect on operation
						1	The op	eration i	s started by the fall	ing edge of TRG
					<b>_</b>	EGS1	ŀ	Hardwar	e trigger enable bit	1
						0	The ris	ing edge	e of TRG has no eff	ect on operation
						1	The op	eration i	s started by the risi	ng edge of TRG

#### Figure 17.5-6 16-bit PPG Status Control Register, Lower Byte (PCNTL0)

#### Table 17.5-2 16-bit PPG Status Control Register, Lower Byte (PCNTL0)

Bit name		Function									
bit7	EGS1: Hardware trigger enable bit1	This bit determines whether to allow or disallow the falling edge of TRG input to stop operation. <b>When the bit is set to ''0''</b> , the falling edge of TRG has no effect on operation. <b>When the bit is set to ''1''</b> , the operation is stopped by the falling edge of TRG.									
bit6	EGS0: Hardware trigger enable bit0	This Wh Wh	This bit determines whether to allow or disallow the rising edge of TRG input to start operation. <b>When the bit is set to "0"</b> , the rising edge of TRG has no effect on operation. <b>When the bit is set to "1"</b> , the operation is started by the rising edge of TRG.								
bit5	IREN: PPG interrupt request enable bit	This Wh Wh	This bit enables or disables PPG interrupt request to the interrupt controller. When the bit is set to "0", an interrupt request is disabled. When the bit is set to "1", an interrupt request is enabled.								
bit4	IRQF: PPG interrupt flag bit	This bit is set to "1" when a PPG interrupt occurs. When the bit is set to "0", clears the bit. When the bit is set to "1", has no effect on operation. "1" is always read in read-modify-write (RMW) instruction.									
	IRS1, IRS0: Interrupt type select bits	The	se bits selec	t the interru	apt type for the PPG timer. Type of interrupt						
								0	0	Trigger by TRG input, software trigger, or retrigger	
bit3			0	1	Counter borrow						
bit2			1	0	Rising edge of PPG output in normal polarity, or falling edge of PPG output in inverted polarity						
				1	1	Counter borrow, rising edge of PPG output in normal polarity, or falling edge of PPG output in inverted polarity					
bit1	POEN: Output enable bit	This bit enables or disables output from the PPG output pin. When the bit is set to "0", the pin serves as a general-purpose port. When the bit is set to "1", the pin serves as the PPG timer output pin.									
bit0	OSEL: Output inversion bit	This bit selects the polarity of PPG output pin. When the bit is set to "0", the PPG output goes to "H" when "L" is output in the internal start and the 16-bit down-counter value matches the duty setting register value, and goes to "L" when a down- counter borrow occurs (Normal polarity). When the bit is set to "1", the PPG output is inverted (Inverted polarity).									

## 17.6 Interrupts of 16-bit PPG Timer

The 16-bit PPG timer can generate interrupt requests in the following cases:

- · When a trigger or counter borrow occurs
- · When a rising edge of PPG is generated in normal polarity
- When a falling edge of PPG is generated in inverted polarity

The interrupt operation is controlled by IRS1 (bit 3) and IRS0 (bit2) in the PCNTL register.

#### Interrupts of 16-bit PPG Timer

Table 17.6-1 shows interrupt control bits and interrupt sources of the 16-bit PPG timer.

Table 17.6-1	Interrupt Control Bit	s and Interrupt S	Sources of 16-bit	<b>PPG</b> Timer

Item	Description				
Interrupt flag bit	PCNTL0:IRQF				
Interrupt request enable bit	PCNTL0:IREN				
Interrupt type select bits	PCNTL0:IRS1, 0				
	PCNTL0:IRS1, 0=00 Hardware trigger by TRG Pin input of 16-bit down-counter, software trigger and retrigger				
	PCNTL0:IRS1, 0=01 Counter borrow of 16-bit down-counter				
Interrupt sources	PCNTL0:IRS1, 0=10 Rising edge of PPG0 output in normal polarity, or falling edge of PPG0 output in inverted polarity				
	PCNTL0:IRS1, 0=11 Counter borrow of 16-bit down-counter, rising edge of PPG0 output in normal polarity, or falling edge of PPG0 output in inverted polarity				

When IRQF (bit 4) in the 16-bit PPG status control register (PCNTL0) is set to "1" and interrupt requests are enabled (PCNTL0:IREN: bit 5 = 1) in the 16-bit PPG timer, an interrupt request is generated and outputted to the controller.

#### ■ Registers and Vector Table Related to Interrupts of 16-bit PPG Timer

#### Table 17.6-2 Registers and Vector Table Related to Interrupts of 16-bit PPG Timer

Interrupt source	Interrupt request No.	Interrupt level	setting register	Vector table address		
		Register	Setting bit	Upper	Lower	
ch.0	IRQ15	ILR3	L15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	

ch.: Channel

Refer to "APPENDIX B Table of Interrupt Causes" for the interrupt request numbers and vector tables of all peripheral functions.

## 17.7 Explanation of 16-bit PPG Timer Operations and Setup Procedure Example

The 16-bit PPG timer can operate in PWM mode or one-shot mode. In addition, a retrigger function can be used in the 16-bit PPG timer.

#### ■ PWM Mode (MDSE of PCNTH Register: bit 5 = 0)

In PWM operation mode, the 16-bit PPG cycle setting buffer register (PCSRH0, PCSRL0) values are loaded and the 16-bit down-counter starts down-count operation when a software trigger is inputted or a hardware trigger by TRG pin input is inputted. When the count value reaches "1", the 16-bit PPG cycle setting buffer register (PCSRH0, PCSRL0) values are reloaded to repeat the down-count operation.

The initial state of the PPG output is "L". When the 16-bit down-counter value matches the value set in the duty setting registers, the output changes to "H" synchronizing with count clock. The output changes back to "L" when the "H" was output until the value of duty setting. (The output levels will be reversed if OSEL is set to "1".)

When the retrigger function is disabled (RTRG = 0), software triggers (STRG = 1) are ignored during the operation of the down-counter.

When the down-counter is not running, the maximum time between a valid trigger input occurring and the down-counter starting is as follows.

Software trigger: 1count clock cycle + 2 machine clock cycles

Hardware trigger by TRG Pin input: 1 count clock cycle + 3 machine clock cycles

The minimum time is as follows.

Software trigger: 2 machine clock cycles

Hardware trigger by TRG Pin input: 3 machine clock cycles

When the down-counter is running, the maximum time between a valid retrigger input occurring and the down-counter restarting is as follows.

Software trigger: 1 count clock cycle + 2 machine clock cycles

Hardware trigger by TRG Pin input: 1 count clock cycle + 3 machine clock cycles

The minimum time is as follows.

Software trigger: 2 machine clock cycles

Hardware trigger by TRG Pin input: 3 machine clock cycles
• Invalidating the retrigger (RTRG of PCNTH0 register: bit 4 = 0)





• Validating the retrigger (RTRG of PCNTH0 register: bit 4 = 1)





## ■ One-shot Mode (MDSE of PCNTH0 Register: bit 5 = 1)

One-shot operation mode can be used to output a single pulse with a specified width when a valid trigger input occurs. When retriggering is enabled and a valid trigger is detected during the counter operation, the down counter value is reloaded.

The initial state of the PPG output is "L". When the 16-bit down-counter value matches the value set in the duty setting registers, the output changes to "H". The output changes back to "L" when the counter reaches "1". (The output levels will be reversed if OSEL is set to 1.)

Invalidating the retrigger (RTRG of PCNTH0 register: bit 4 = 0)



#### Figure 17.7-3 When Retrigger Is Invalid in One-shot Mode

Validating the retrigger (RTRG of PCNTH0 register: bit 4 = 1)



#### Figure 17.7-4 When Retrigger Is Valid in One-shot Mode

## Hardware Trigger

"Hardware trigger" refers to PPG activation by signal input to the TRG input pin. When EGS1 and EGS0 are set to " $11_B$ " and the hardware trigger is used with TRG input, PPG starts operation on a rising edge and halts the operation upon the detection of a falling edge.

Moreover, the PPG timer begins operation of the following rising edge from the beginning.

The operation can be retriggered by a valid TRG input hardware trigger regardless of the retrigger setting of the RTRG bit when the TRG input hardware trigger has been selected.





## Setup Procedure Example

The 16-bit PPG timer is set up in the following procedure:

#### Initial setup

- 1) Set the interrupt level (ILR3, ILR4)
- 2) Enable the hardware trigger and interrupts, select the interrupt type, and enable output (PCNTL)
- 3) Select the count clock and the mode, and enable timer operation (PCNTH)
- 4) Set the cycle (PCSR)
- 5) Set the duty (PDUT)
- 6) Start the PPG by the software trigger (PCNTH:STGR = 1)

#### Interrupt processing

- 1) Process any interrupt
- 2) Clear the interrupt request flag (PCNTL:IRQF)

## 17.8 Precautions when Using 16-bit PPG Timer

## Shown below are the precautions that must be followed when using the 16-bit PPG timer.

## Precautions when Using 16-bit PPG Timer

#### Precautions when setting the program

Do not use the retrigger if the same values are set for the cycle and duty. If used, the PPG output will go to the "L" level for one count clock cycle after the retrigger, and then go back to the "H" level when normal polarity has been selected.

If the microcontroller enters a standby mode, the TRG pin setting may change and cause the device to malfunction. Therefore, disable the timer enable bit (PCNTH0:CNTE = 0) or disable the hardware trigger enable bit (PCNTL0:EGS1, EGS0 =  $00_B$ ).

When the cycle and duty are set to the same value, an interrupt is generated only once by duty match. Moreover, if the duty is set to a value greater than the value of the period, no interrupt will be generated by duty match.

Do not disable the timer enable bit (PCNTH0: CNTE = 0) and software trigger (PCNTH0: STRG = 1) at the same time when retrigger by the software is enabled (PCNTH0: RTRG = 1) and the retrigger is selected as an interrupt type (PCNTL0: IRS1, IRS0 =  $00_B$ ) during count operation. If it occurs, interrupt flag bit may set by retrigger although timer stops.

## 17.9 Sample Programs for 16-bit PPG Timer

## We provide sample programs that can be used to operate the 16-bit PPG timer.

## ■ Sample Programs for 16-bit PPG Timer

For information about the sample programs for the 16-bit PPG timer, refer to "■ Sample Programs" in Preface.

## Setup Methods without Sample Program

• How to set the PPG operation mode

The operation mode select bit (PCNTH0:MDSE) is used.

Operation mode	Operation mode select bit (MDSE)
PWM mode	Set the bit to "0"
One-shot mode	Set the bit to "1"

• How to select the operating clock

The operating clock select bits (PCNTH0:CKS2/CKS1/CKS0) are used to select the clock.

## • How to enable/disable the PPG output pin

The output enable bit (PCNTL0:POEN) is used.

What to be controlled	Output enable bit (POEN)
When enabling PPG output	Set the bit to "1"
When disabling PPG output	Set the bit to "0"

• How to enable/disable PPG operation

The timer enable bit (PCNTH0:CNTE) is used.

What to be controlled	Timer enable bit (CNTE)
When disabling PPG operation	Set the bit to "0"
When enabling PPG operation	Set the bit to "1"

Enable PPG operation before starting the PPG.

#### • How to start PPG operation by software

The software trigger bit (PCNTH0:STGR) is used.

What to be controlled	Software trigger bit (STGR)
When starting PPG operation by software	Set the bit to "1"

• How to enable/disable the retrigger function of the software trigger

The retrigger enable bit (PCNTH0:RTRG) is used.

What to be controlled	Retrigger enable bit (RTRG)
When enabling retrigger function	Set the bit to "1"
When disabling retrigger function	Set the bit to "0"

• How to start/stop operation on a rising edge of trigger input

The hardware trigger enable bit (PCNTH0:EGS0) is used.

What to be controlled	Hardware trigger enable bit (EGS0)
When starting operation on rising edge	Set the bit to "1"
When stopping operation on rising edge	Set the bit to "0"

• How to start/stop operation on a falling edge of trigger input

The hardware trigger enable bit (PCNTH0:EGS1) is used.

What to be controlled	Hardware trigger enable bit (EGS1)
When starting operation on falling edge	Set the bit to "1"
When stopping operation on falling edge	Set the bit to "0"

#### • How to invert PPG output

The output inversion bit (PCNTL0:OSEL) is used.

What to be controlled	Output inversion bit (OSEL)
When inverting PPG output	Set the bit to "1"

#### • How to set the PPG output to the "H" or "L" level

The PPG output mask enable bit (PCNTH0:PGMS) and the output inversion bit (PCNTL0:OSEL) are used.

What to be controlled	PPG output mask enable bit (PGMS)	Output inversion bit (OSEL)
When setting output to "H" level	Set the bit to "1"	Set the bit to "1"
When setting output to "L" level	Set the bit to "1"	Set the bit to "0"

#### How to select the interrupt source

The interrupt select bits (PCNTL0:IRS1/IRS0) are used to select the interrupt source.

Interrupt source	Interrupt select bits (IRS1/IRS0)
Trigger by TRG input, software trigger, or retrigger	Set the bits to "00 <sub>B</sub> "
Counter borrow	Set the bits to "01 <sub>B</sub> "
Rising edge of PPG output in normal polarity, or falling edge of PPG output in inverted polarity	Set the bits to "10 <sub>B</sub> "
Counter borrow, rising edge of PPG output in normal polarity, or falling edge of PPG output in inverted polarity	Set the bits to "11 <sub>B</sub> "

#### Interrupt-related registers

The interrupt level is set by the level setting registers shown in the following table.

Interrupt source	Interrupt level setting register	Interrupt vector
ch.0	Interrupt level register (ILR3) Address: 0007C <sub>H</sub>	#15 Address: 0FFDC <sub>H</sub>

#### • How to enable/disable/clear interrupts

The interrupt request enable bit (PCNTL0:IREN) is used to enable interrupts.

What to be controlled	Interrupt request enable bit (IREN)
When disabling interrupt request	Set the bit to "0"
When enabling interrupt request	Set the bit to "1"

The interrupt request flag (PCNTL0:IRQF) is used to clear interrupt requests.

What to be controlled	Interrupt request flag (IRQF)
When clearing interrupt request	Write "0" to the bit

## CHAPTER 17 16-BIT PPG TIMER

# CHAPTER 18 EXTERNAL INTERRUPT CIRCUIT

This chapter describes the functions and operations of the external interrupt circuit.

- 18.1 Overview of External Interrupt Circuit
- 18.2 Configuration of External Interrupt Circuit
- 18.3 Channels of External Interrupt Circuit
- 18.4 Pins of External Interrupt Circuit
- 18.5 Registers of External Interrupt Circuit
- 18.6 Interrupts of External Interrupt Circuit
- 18.7 Explanation of External Interrupt Circuit Operations and Setup Procedure Example
- 18.8 Precautions when Using External Interrupt Circuit
- 18.9 Sample Programs for External Interrupt Circuit

## **18.1** Overview of External Interrupt Circuit

The external interrupt circuit detects edges on the signal that is inputted to the external interrupt pin and generates interrupt requests to the CPU.

## Functions of External Interrupt Circuit

The external interrupt circuit has the functions to detect any edge of a signal that is inputted to an external interrupt pin and generate an interrupt request to the CPU. This interrupt allows the unit to recover from a standby mode and return to its normal operation.

## 18.2 Configuration of External Interrupt Circuit

The external interrupt circuit consists of the following blocks:

- Edge detection circuit
- External interrupt control register

## Block Diagram of External Interrupt Circuit

Figure 18.2-1 shows the block diagram of the external interrupt circuit.



#### Figure 18.2-1 Block Diagram of External Interrupt Circuit (Unit0)

## Edge detection circuit

When the polarity of the edge detected on a signal inputted to an external interrupt circuit pin (INT) matches the polarity of the edge selected in the interrupt control register (EIC), the corresponding external interrupt request flag bit (EIR) is set to "1".

## External interrupt control register (EIC)

This register is used to select the valid edge, enable or disable interrupt requests, check for interrupt requests, etc.

## **18.3 Channels of External Interrupt Circuit**

## This section describes the channels of the external interrupt circuit.

## ■ Channels of External Interrupt Circuit

In MB95130/M series, each unit has four channels of the external interrupt circuit. Table 18.3-1 and Table 18.3-2 show the correspondence among the channel, pin and register.

Unit	Pin name	Pin function
0	INT00	External interrupt input ch.0
	INT01	External interrupt input ch.1
1	INT02	External interrupt input ch.2
	INT03	External interrupt input ch.3
2	INT04	External interrupt input ch.4
2	INT05	External interrupt input ch.5
3	INT06	External interrupt input ch.6
	INT07	External interrupt input ch.7

Table 18.3-1 Pins of External Interrupt Circuit

#### Table 18.3-2 Registers of External Interrupt Circuit

Unit	Register name	Corresponding register (Name in this manual)
0	EIC00	
1	EIC10	FIC: External Interrupt Control register
2	EIC20	ERC. External interrupt Control register
3	EIC30	

The following sections only describe the unit 0 side of the external interrupt circuit.

The other units are the same as the unit 0 side of the external interrupt circuit.

## 18.4 Pins of External Interrupt Circuit

# This section shows the pins related to the external interrupt circuit and the block diagram of such pins.

## Pins Related to External Interrupt Circuit

The pins related to the external interrupt circuit are the INT00 to INT07 pins.

• INT00 to INT07 pins

These pins serve both as external interrupt inputs and as general-purpose I/O ports.

INT00 to INT07: When the corresponding pin of the INT00 to INT07 pins is set as an input port by the port direction register (DDR) and the corresponding external interrupt input is enabled by the external interrupt control register (EIC), that pin functions as an external interrupt input pin (INT00 = INT07). The state of pins can be read from the port data register (PDR) whenever input port is set as a pin function. However, the value of PDR is read when read-modify-write

(RMW) instruction is used.

## Block Diagram of Pins Related to External Interrupt Circuit





## 18.5 Registers of External Interrupt Circuit

## This section describes the registers of the external interrupt circuit.

## ■ List of Registers of External Interrupt Circuit

Figure 18.5-1 shows the registers of the external interrupt circuit.

,W R/W bit6	SL10 R/W	EIE1 R/W	EIR0 R(RM1),W	SL01	SL00	EIE0	00000000 <sub>B</sub>
,w R/W bit6	R/W	R/W	R(RM1),W				
bit6				r/w	R/W	R/W	
	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0	00000000 <sub>B</sub>
,W R/W	R/W	R/W	R(RM1),W	R/W	R/W	R/W	2
bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0	00000000 <sub>B</sub>
,w R/W	R/W	R/W	R(RM1),W	R/W	R/W	R/W	1
bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
SL11	SL10	EIE1	EIR0	SL01	SL00	EIE0	00000000 <sub>B</sub>
W R/W	R/W	R/W	R(RM1) W		D/\//	P/\//	1
	,W     R/W       bit6       I     SL11       ,W     R/W       bit6       I     SL11       .W     Bit6       I     SL11	W     R/W     R/W       bit6     bit5       I     SL11     SL10       ,W     R/W     R/W       bit6     bit5       I     SL11     SL10       ,W     R/W     Dit5	W     R/W     R/W     R/W       bit6     bit5     bit4       I     SL11     SL10     EIE1       .W     R/W     R/W     R/W       bit6     bit5     bit4       I     SL11     SL10     EIE1       .W     R/W     R/W     EIE1       .W     SL11     SL10     EIE1	W     R/W     R/W     R/W     R(RM1),W       bit6     bit5     bit4     bit3       I     SL11     SL10     EIE1     EIR0       ,W     R/W     R/W     R/W     R(RM1),W       bit6     bit5     bit4     bit3       I     SL11     SL10     EIE1     EIR0       ,W     R/W     R/W     R/W     R(RM1),W       bit6     bit5     bit4     bit3       I     SL11     SL10     EIE1     EIR0       W     SW     SUM     SUM     S(M)	W     R/W     R/W     R/W     R/W     R/W       bit6     bit5     bit4     bit3     bit2       I     SL11     SL10     EIE1     EIR0     SL01       ,W     R/W     R/W     R/W     R(M1),W     R/W       bit6     bit5     bit4     bit3     bit2       I     SL11     SL10     EIE1     EIR0     SL01       ,W     R/W     R/W     R/W     R(M1),W     R/W       bit6     bit5     bit4     bit3     bit2       I     SL11     SL10     EIE1     EIR0     SL01	.W     R/W     R/W     R/W     R/W     R/W       bit6     bit5     bit4     bit3     bit2     bit1       I     SL11     SL10     EIE1     EIR0     SL01     SL00       .W     R/W     R/W     R/W     R/W     R/W     R/W       bit6     bit5     bit4     bit3     bit2     bit1       I     SL11     SL10     EIE1     EIR0     SL01     SL00       .W     R/W     R/W     R/W     R/W     R/W     R/W       bit6     bit5     bit4     bit3     bit2     bit1       I     SL11     SL10     EIE1     EIR0     SL01     SL00	

## Figure 18.5-1 Registers of External Interrupt Circuit

## 18.5.1 External Interrupt Control Register (EIC00)

The external interrupt control register (EIC00) is used to select the edge polarity for the external interrupt input and control interrupts.

## External Interrupt Control Register (EIC00)

Address	S	bit7	b	oit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	
0048н 0049н	EIC00 EIC10	EIR	I S	L11	SL10	EIE1	EIR0	SL01	SL00	EIEC	) 00000000 <sub>В</sub>	
004Ан 004Вн	EIC20 EIC30	R(RM1)	),W R	./W	R/W	R/W	R(RM1),W	′ R/W	R/W	R/W		
						EIEU		Diec	Interrupt	reque	st enable bit U	
						1		Ena	bles out	nut of	interrupt request	
						-		Liia	0100 001	putor		
						SL01	SL00		Edg	je pola	rity select bits 0	
						0	0		No	o edge	detection	
						0	1			Risin	g edge	
						1	0			Fallin Poth	g edge	
					L	1				DOIN	euges	
					].[			Ext	ternal int	errupt	request flag bit 0	
						EIRU		Read	1		Write	
						0	Specifi	ed edge	not inputte	ed	Clears this bit	
					L	1	Spec	ified edg	e inputted	I N	lo change, no effect on others	
					<b>\</b>	FIF1			Interrunt	ronuo	st enable hit 1	
					-	0		Disa	ables ou	tout of	interrupt request	
						1		Ena	ables ou	tput of	interrupt request	
					-	-						
				L		SL11	SL10		Edg	je pola	rity select bits 1	
					F	0	0		N	o edge	e detection	
					F	1	0			Fallin	y euge	
					-	1	1			Both	edges	
					_							
						EIR1		Ext	ernal int	errupt	request flag bit 1	
								Read	1		Write	
					-	1	Specifi	ed edge	not inputted	ed	Clears this bit	
					L	I	Spec	illea eag	emputed	i ľ	NO GHANGE, NO ENECT ON OTHERS	
P/M	. 🗆	adable	/writa	hla (P		is the cr	amo ao writ	(میراور م				
R(RM	11),W : R : Ir	leadable	e/writa Je	ble (R	ead value	is differe	ent from wr	ite value,	, "1" is rea	ld by rea	ad-modify-write (RMW) instruction)	

## Figure 18.5-2 External Interrupt Control Register (EIC00)

	Bit name	Function
bit7	EIR1: External interrupt request flag bit 1	<ul> <li>This flag is set to "1" when the edge selected by the edge polarity select bits (SL11, SL10) is inputted to the external interrupt pin INT1.</li> <li>When this bit and the interrupt request enable bit 1 (EIE1) are set to "1", an interrupt request is outputted.</li> <li>Writing "0" clears the bit. Writing "1" has no effect.</li> <li>"1" is read in read-modify-write (RMW) instructions.</li> </ul>
bit6 bit5	SL11, SL10: Edge polarity select bits 1	<ul> <li>These bits select the polarity of the interrupt source edge of the pulse inputted to the external interrupt pin INT1.</li> <li>Edge detection is not performed and no interrupt is generated when these bits are set to "00<sub>B</sub>".</li> <li>Rising edges are detected when these bits are "01<sub>B</sub>", falling edges when "10<sub>B</sub>", and both edges when "11<sub>B</sub>".</li> </ul>
bit4	EIE1: Interrupt request enable bit 1	<ul> <li>This bit is used to enable and disable output of interrupt requests to the interrupt controller. When this bit and the external interrupt request flag bit 1 (EIR1) are "1", an interrupt request is outputted.</li> <li>When using an external interrupt pin, write "0" to the corresponding bit in the port direction register (DDR) to set the pin as an input.</li> <li>The status of the external interrupt pin can be read directly from the port data register, regardless of the status of the interrupt request enable bit.</li> </ul>
bit3	EIR0: External interrupt request flag bit 0	<ul> <li>This flag is set to "1" when the edge selected by the edge polarity select bits (SL01, SL00) is inputted to the external interrupt pin INTO.</li> <li>When this bit and the interrupt request enable bit 0 (EIE0) are set to "1", an interrupt request is outputted.</li> <li>Writing "0" clears the bit. Writing "1" has no effect.</li> <li>"1" is read in read-modify-write (RMW) instructions.</li> </ul>
bit2 bit1	SL01, SL00: Edge polarity select bits 0	<ul> <li>These bits are used to select the polarity of the interrupt source edge of the pulse inputted to the external interrupt pin INTO.</li> <li>Edge detection is not performed and no interrupt request is generated when these bits are "00<sub>B</sub>".</li> <li>Rising edges are detected when the bits are "01<sub>B</sub>", falling edges when "10<sub>B</sub>", and both edges when "11<sub>B</sub>".</li> </ul>
bit0	EIE0: Interrupt request enable bit 0	<ul> <li>This bit enables or disables the output of interrupt requests to the interrupt controller. An interrupt request is outputted when this bit and the external interrupt request flag bit 0 (EIR0) are "1".</li> <li>When using an external interrupt pin, write "0" to the corresponding bit in the port direction register (DDR) to set the pin as an input.</li> <li>The status of the external interrupt pin can be read directly from the port data register (PFR), regardless of the status of the interrupt request enable bit.</li> </ul>

Table 18.5-1 Functional Description of Each Bit of External Interrupt Control Register (EIC00)

## 18.6 Interrupts of External Interrupt Circuit

# The interrupt sources for the external interrupt circuit include detection of the specified edge of the signal inputted to an external interrupt pin.

## ■ Interrupt During Operation of External Interrupt Circuit

When the specified edge of external interrupt input is detected, the corresponding external interrupt request flag bit (EIC: EIR0, EIR1) is set to "1". In this case, an interrupt request will be generated to the interrupt controller, if the corresponding interrupt request enable bit is enabled (EIC: EIE0, EIE1=1). Write "0" to the corresponding external interrupt request flag big to clear the interrupt request in the interrupt process routine.

## ■ Registers and Vector Table Related to Interrupts of External Interrupt Circuit

Interrupt	Interrupt	Interrupt level	setting register	Vector table address		
source	request No.	Register	Setting bit	Upper	Lower	
ch.0	IROO	II RO	1.00	FFFA	FFFB.	
ch.4	тQU	ILKO	LOO	I I I I H	$111D_{\rm H}$	
ch.1	IRO1	II RO	I 01	FFF8 <sub>11</sub>	FFF9.	
ch.5	ikųr	ILKO	LOI	IIIOH	III /H	
ch.2	IRO2	II RO	1.02	FFF6	FFF7	
ch.6	IKQ2	ILKO	LOZ	III 0H	H /H	
ch.3	IRO3	II RO	1.03	FFF4.	FFF5.	
ch.7	ing5	ILKO	205	··· TH	····· <sup>H</sup>	

#### Table 18.6-1 Registers and Vector Table Related to Interrupts of External Interrupt Circuit

ch.: Channel

Refer to "APPENDIX B Table of Interrupt Causes" for the interrupt request numbers and vector tables of all peripheral functions.

## 18.7 Explanation of External Interrupt Circuit Operations and Setup Procedure Example

## This section describes the operation of the external interrupt circuit.

## Operation of External Interrupt Circuit

When the polarity of an edge of a signal inputted from one of the external interrupt pins (INT0, 1) matches the polarity of the edge selected by the external interrupt control register (EIC: SL00 to SL11), the corresponding external interrupt request flag bit (EIC: EIR0, EIR1) is set to "1" and the interrupt request is generated.

Always set the interrupt enable bit to "0" when not using an external interrupt to recover from a standby mode.

When setting the edge polarity select bit (SL), set the interrupt request enable bit (EIE) to "0" to prevent the interrupt request from being generated accidentally. Also clear the interrupt request flag bit (EIR) to "0" after changing the edge polarity.

Figure 18.7-1 shows the operation for setting the INT0 pin as an external interrupt input.



Figure 18.7-1 Operation of External Interrupt

## Setup Procedure Example

The external interrupt circuit is set up in the following procedure:

- Initial setup
  - 1) Set the interrupt level. (ILR0)
  - 2) Select the edge polarity. (EIC:SL01, SL00)
  - 3) Enable interrupt requests. (EIC:EIE0 = 1)

#### Interrupt processing

- 1) Clear the interrupt request flag. (EIC:EIR0 = 0)
- 2) Process any interrupt.

#### Note:

The external interrupt input is also used as an I/O port. Therefore, when it is used as the external interrupt input, the corresponding bit in the port direction register (DDR) must be set to "0" (input).

## **18.8** Precautions when Using External Interrupt Circuit

## This section describes the precautions that must be followed when using the external interrupt circuit.

## Precautions when Using External Interrupt Circuit

- Set the interrupt request enable bit (EIE) to "0" (disabling interrupt requests) when setting the edge polarity select bit (SL). Also clear the external interrupt request flag bit (EIR) to "0" after setting the edge polarity.
- The operation cannot recover from the interrupt processing routine if the external interrupt request flag bit is "1" and the interrupt request enable bit is enabled. Always clear the external interrupt request flag bit in the interrupt processing routine.

## **18.9** Sample Programs for External Interrupt Circuit

## We provide sample programs that can be used to operate the external interrupt circuit.

## ■ Sample Programs for External Interrupt Circuit

For information about the sample programs for the external interrupt circuit, refer to " Sample Programs" in Preface.

## Setup Methods without Sample Program

• Detection levels and setup methods

Four detection levels are available: no edge detection, rising edge, falling edge, both edges The detection level bits (EIC: SL01, SL00 or EIC: SL11, SL10) are used.

Operation mode	Detection level bits (SL01,SL00)
No edge detection	Select "00 <sub>B</sub> "
Detecting rising edges	Select "01 <sub>B</sub> "
Detecting falling edges	Select "10 <sub>B</sub> "
Detecting both edges	Select "11 <sub>B</sub> "

How to use the external interrupt pin

Set the corresponding data direction register (DDR0) to "0".

Operation	Direction bit (P00 to P07)	Setting
Using INT00 pin for external interrupt	DDR0: P00	Set the register to "0"
Using INT01 pin for external interrupt	DDR0: P01	Set the register to "0"
Using INT02 pin for external interrupt	DDR0: P02	Set the register to "0"
Using INT03 pin for external interrupt	DDR0: P03	Set the register to "0"
Using INT04 pin for external interrupt	DDR0: P04	Set the register to "0"
Using INT05 pin for external interrupt	DDR0: P05	Set the register to "0"
Using INT06 pin for external interrupt	DDR0: P06	Set the register to "0"
Using INT07 pin for external interrupt	DDR0: P07	Set the register to "0"

#### Interrupt-related registers

The interrupt level is set by the interrupt level setting registers shown in the following table.

	Interrupt level setting register	Interrupt vector
ch.0	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#0 Address: 0FFFA <sub>H</sub>
ch.1	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#1 Address: 0FFF8 <sub>H</sub>
ch.2	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#2 Address: 0FFF6 <sub>H</sub>
ch.3	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#3 Address: 0FFF4 <sub>H</sub>
ch.4	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#0 Address: 0FFFA <sub>H</sub>
ch.5	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#1 Address: 0FFF8 <sub>H</sub>
ch.6	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#2 Address: 0FFF6 <sub>H</sub>
ch.7	Interrupt level register (ILR0) Address: 00079 <sub>H</sub>	#3 Address: 0FFF4 <sub>H</sub>

• How to enable/disable/clear interrupts

Interrupts are enabled by the interrupt enable bit (EIC00: EIE0 or EIE1).

What to be controlled	Interrupt enable bit (EIE0 or EIE1)
When disabling interrupt request	Set the bit to "0"
When enabling interrupt request	Set the bit to "1"

Interrupt requests are cleared by the interrupt request bit (EIC00: EIR0 or EIR1).

What to be controlled	Interrupt request bit (EIR0 or EIR1)
When clearing interrupt request	Write "0"

# CHAPTER 19 INTERRUPT PIN SELECTION CIRCUIT

This chapter describes the functions and operations of the interrupt pin selection circuit.

- 19.1 Overview of Interrupt Pin Selection Circuit
- 19.2 Configuration of Interrupt Pin Selection Circuit
- 19.3 Pins of Interrupt Pin Selection Circuit
- 19.4 Registers of Interrupt Pin Selection Circuit
- 19.5 Operating Description of Interrupt Pin Selection Circuit
- 19.6 Precautions when Using Interrupt Pin Selection Circuit

## **19.1** Overview of Interrupt Pin Selection Circuit

# The interrupt pin selection circuit selects pins to be used as interrupt input pins from among various peripheral input pins.

## ■ Interrupt Pin Selection Circuit

The interrupt pin selection circuit is used to select interrupt input pins from amongst various peripheral inputs (TRG0/ADTG, UCK0, UI0, EC0, SCK, SI, INT00). The input signal from each peripheral function pin is selected by this circuit and the signal is used as the INT00 (channel 0) input of external interrupt. This enables the input signals to the peripheral function pins to also serve as external interrupt pins.

## **19.2** Configuration of Interrupt Pin Selection Circuit

Figure 19.2-1 shows the block diagram of the interrupt pin selection circuit.

## ■ Block Diagram of Interrupt Pin Selection Circuit



## Figure 19.2-1 Block Diagram of Interrupt Pin Selection Circuit

• WICR register (interrupt pin selection circuit control register)

This register is used to determine which of the available peripheral input pins should be outputted to the interrupt circuit and which interrupt pins they should serve as.

Selection circuit

This circuit outputs the input from the pin selected by the WICR register to the INT00 input of the external interrupt circuit (ch.0).

## **19.3** Pins of Interrupt Pin Selection Circuit

## This section describes the pins of the interrupt pin selection circuit.

## ■ Pins Related to Interrupt Pin Selection Circuit

The peripheral function pins related to the interrupt pin selection circuit are the TRG0/ADTG, UCK0, UI0, EC0, SCK, SI, and INT00 pins. These inputs (except INT00) are also connected to their respective peripheral units in parallel and can be used for both functions simultaneously. Table 19.3-1 lists the correlation between the peripheral functions and peripheral input pins.

Table 19.3-1	Correlation	Between	Peripheral	Functions	and Peri	pheral In	put Pins
							4

Peripheral input pin name	Peripheral functions name
INT00	Interrupt pin selection circuit
TRG0/ ADTG	Interrupt pin selection circuit 16-bit PPG timer (trigger input) 8/10-bit A/D converter (trigger input)
UCK0	Interrupt pin selection circuit UART/SIO (clock input/output)
UIO	Interrupt pin selection circuit UART/SIO (data input)
EC0	Interrupt pin selection circuit 8/16-bit compound timer (event input)
SCK	Interrupt pin selection circuit LIN-UART (clock input/output)
SI	Interrupt pin selection circuit LIN-UART (data input)

## **19.4 Registers of Interrupt Pin Selection Circuit**

Figure 19.4-1 shows the registers related to the interrupt pin selection circuit.

## ■ Registers Related to Interrupt Pin Selection Circuit

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FEF <sub>H</sub>	-	INT00	SI	SCK	EC0	UIO	UCK0	TRG0	01000000 <sub>B</sub>
	R0/WX	R/W	R/W	R/W	R/W	R/W	R/W	R/W	_

## **19.4.1** Interrupt Pin Selection Circuit Control Register (WICR)

This register is used to determine which of the available peripheral input pins should be outputted to the interrupt circuit and which interrupt pins they should serve as.

## ■ Interrupt Pin Selection Circuit Control Register (WICR)



#### Figure 19.4-2 Interrupt Pin Selection Circuit Control Register (WICR)

Bit name		Function
bit7	Unused bit	<ul><li>This bit is not used.</li><li>Reading always returns "0".</li><li>Writing has no effect on the operation.</li></ul>
bit6	INT00: IINT00 interrupt pin select bit	This bit is used to determine whether to select the INT00 pin as an interrupt input pin. <b>Writing ''0'</b> ' to the bit deselects the INT00 pin as an interrupt input pin and the circuit treats the INT00 pin input as being fixed at "0". <b>Writing ''1''</b> to the bit selects the INT00 pin as an interrupt input pin and the circuit passes the INT00 pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the INT00 pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.
bit5	SI: SI interrupt pin select bit	<ul> <li>This bit is used to determine whether to select the SI pin as an interrupt input pin.</li> <li>Writing "0" to the bit deselects the SI pin as an interrupt input pin and the circuit treats the SI pin input as being fixed at "0".</li> <li>Writing "1" to the bit selects the SI pin as an interrupt input pin and the circuit passes the SI pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the SI pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.</li> </ul>
bit4	SCK: SCK interrupt pin select bit	This bit is used to determine whether to select the SCK pin as an interrupt input pin. <b>Writing ''0'</b> ' to the bit deselects the SCK pin as an interrupt input pin and the circuit treats the SCK pin input as being fixed at "0". <b>Writing ''1''</b> to the bit selects the SCK pin as an interrupt input pin and the circuit passes the SCK pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the SCK pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.
bit3	EC0: EC0 interrupt pin select bit	This bit is used to determine whether to select the EC0 pin as an interrupt input pin. <b>Writing "0"</b> to the bit deselects the EC0 pin as an interrupt input pin and the circuit treats the EC0 pin input as being fixed at "0". <b>Writing "1"</b> to the bit selects the EC0 pin as an interrupt input pin and the circuit passes the EC0 pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the EC0 pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.
bit2	UI0: UI0 interrupt pin select bit	This bit is used to determine whether to select the UI0 pin as an interrupt input pin. Writing "0" to the bit deselects the UI0 pin as an interrupt input pin and the circuit treats the UI0 pin input as being fixed at "0". Writing "1" to the bit selects the UI0 pin as an interrupt input pin and the circuit passes the UI0 pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the UI0 pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.
bit1	UCK0: UCK0 interrupt pin select bit	This bit is used to determine whether to select the UCK0 pin as an interrupt input pin. <b>Writing ''0'</b> ' to the bit deselects the UCK0 pin as an interrupt input pin and the circuit treats the UCK0 pin input as being fixed at "0". <b>Writing ''1''</b> to the bit selects the UCK0 pin as an interrupt input pin and the circuit passes the UCK0 pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the UCK0 pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.
bit0	TRG0: TRG0 interrupt pin select bit	This bit is used to determine whether to select the TRG0 pin as an interrupt input pin. <b>Writing ''0'</b> ' to the bit deselects the TRG0 pin as an interrupt input pin and the circuit treats the TRG0 pin input as being fixed at "0". <b>Writing ''1''</b> to the bit selects the TRG0 pin as an interrupt input pin and the circuit passes the SCK pin input to INT00 (ch.0) of the external interrupt circuit. In this case, the input signal to the SCK pin can generate an external interrupt if INT00 (ch.0) operation is enabled in the external interrupt circuit.

## Table 19.4-1 Functional Description of Each Bit of Interrupt Pin Selection Circuit Control Register (WICR)

When these bits are set to "1" and the operation of INT00 (ch.0) of the external interrupt circuit is enabled in MCU standby mode, the selected pins are enabled to perform input operation. The MCU wakes up from the standby mode when a valid edge pulse is inputted to the pins. For information about the standby modes, refer to "6.8 Operations in Low-power Consumption Modes (Standby Modes)".

#### Note:

The input signals to the peripheral pins do not generate an external interrupt even when "1" is written to these bits if the INT00 (ch.0) of the external interrupt circuit is disabled.

Do not modify the values of these bits while the INT00 (ch.0) of the external interrupt circuit is enabled. If modified, the external interrupt circuit may detect a valid edge, depending on the pin input level.

If more than one interrupt pin are selected in WICR (interrupt pin selection circuit control register) simultaneously and the operation of INT00 (ch.0) of the external interrupt circuit is enabled (the values other than " $00_B$ " are set to SL01, SL00 bits in EIC00 register of external interrupt circuit.), the selected pins will remain enabled to perform input so as to accept interrupts even in a standby mode.

## **19.5** Operating Description of Interrupt Pin Selection Circuit

# The interrupt pins are selected by setting WICR (interrupt pin selection circuit control register).

## Operation of Interrupt Pin Selection Circuit

The WICR (interrupt pin selection circuit control register) setting is used to select the input pins to be inputted to INT00 of the external interrupt circuit (ch.0). Shown below is the setup procedure for the interrupt pin selection circuit and external interrupt circuit (ch.0), which must be followed when selecting the TRG0 pin as an interrupt pin.

- 1) Write "0" to the corresponding bit in the port direction register (DDR) to set the pin as an input.
- 2) Select the TRG0 pin as an interrupt input pin in WICR (interrupt pin selection circuit control register) (Write " $01_{\text{H}}$ " to the WICR register. At this point, after writing "0" in the EIE0 bit of the EIC00 register of the external interrupt circuit, the operation of the external interrupt circuit is disabled).
- 3) Enable the operation of INT00 of the external interrupt circuit (ch.0). (Set the SL01 and SL00 bits of the EIC00 register to any value other than " $00_B$ " in the external interrupt circuit to select the valid edge. Also write "1" to the EIE0 bit to enable interrupts).
- 4) The subsequent interrupt operation is the same as for the external interrupt circuit.
- When a reset is released, WICR (interrupt pin selection circuit control register) is initialized to " $40_{\rm H}$ " and the INT00 bit is selected as the only available interrupt pin. Update the value of this register before enabling the operation of the external interrupt circuit, when using any pins other than the INT00 pin as external interrupt pins.

Note:

If more than one interrupt pin are selected in WICR (interrupt pin selection circuit control register) simultaneously, an input to INT00 (ch.0) of the external interrupt circuit is treated as "H" if any of the selected input signals is "H". (It becomes "OR" of the signals inputted to the selected pins.)

## **19.6 Precautions when Using Interrupt Pin Selection Circuit**

# This section explains the precautions to be taken when using the interrupt pin selection circuit.

- If more than one interrupt pin are selected in WICR (interrupt pin selection circuit control register) simultaneously and the operation of INT00 (ch.0) of the external interrupt circuit is enabled (Set the SL01 and SL00 bits of the EIC00 register to any value other than " $00_B$ " in the external interrupt circuit to select the valid edge. Also write "1" to the EIE0 bit to enable interrupts), the selected pins will remain enabled to perform input so as to accept interrupts even in a standby mode.
- If more than one interrupt pin are selected in WICR (interrupt pin selection circuit control register) simultaneously, an input to INT00 (ch.0) of the external interrupt circuit is treated as "H" if any of the selected input signals is "H" (It becomes "OR" of the signals inputted to the selected pins).

# CHAPTER 20 UART/SIO

This chapter describes the functions and operations of UART/SIO.

- 20.1 Overview of UART/SIO
- 20.2 Configuration of UART/SIO
- 20.3 Channels of UART/SIO
- 20.4 Pins of UART/SIO
- 20.5 Registers of UART/SIO
- 20.6 Interrupts of UART/SIO
- 20.7 Explanation of UART/SIO Operations and Setup Procedure Example
- 20.8 Sample Programs for UART/SIO

## 20.1 Overview of UART/SIO

The UART/SIO is a general-purpose serial data communication interface. Serial data transfers of variable-length data can be made with a synchronous or asynchronous clock. The transfer format is NRZ. The transfer rate can be set with the dedicated baud rate generator or external clock (in clock synchronous mode).

## Functions of UART/SIO

The UART/SIO is capable of serial data transmission/reception (serial input/output) to and from another CPU or peripheral device.

- Equipped with a full-duplex double buffer that allows 2-way full-duplex communication.
- The synchronous or asynchronous transfer mode can be selected.
- The optimum baud rate can be selected with the dedicated baud rate generator.
- The data length is variable; it can be set to 5 bit to 8 bit when no parity is used or to 6 bit to 9 bit when parity is used. (Refer to Table 20.1-1.)
- The serial data direction (endian) can be selected.
- The data transfer format is NRZ (Non-Return-to-Zero).
- Two operation modes (operation modes 0 and 1) are available. Operation mode 0 operates as asynchronous clock mode (UART). Operation mode 1 operates as clock synchronous mode (SIO).

#### Table 20.1-1 UART/SIO Operation Modes

Operation mode	Data	length	Synchronization	Length of stop bit	
Operation mode	No parity	With parity	mode	Longin of otop bit	
0	5	6			
	6	7	Asunchronous	1 bit or 2 bits	
	7	8	Asynchronous		
	8	9			
1	5	-			
	6	-	Synchronous		
	7	-	Synchronous	-	
	8	-			

## 20.2 Configuration of UART/SIO

The UART/SIO consists of the following blocks:

- UART/SIO serial mode control register 1 (SMC10)
- UART/SIO serial mode control register 2 (SMC20)
- UART/SIO serial status and data register (SSR0)
- UART/SIO serial input data register (RDR0)
- UART/SIO serial output data register (TDR0)

## Block Diagram of UART/SIO



Figure 20.2-1 Block Diagram of UART/SIO

• UART/SIO serial mode control register 1 (SMC10)

This register controls UART/SIO operation mode. It is used to set the serial data direction (endian), parity and its polarity, stop bit length, operation mode (synchronous/asynchronous), data length, and serial clock.

UART/SIO serial mode control register 2 (SMC20)

This register controls UART/SIO operation mode. It is used to enable/disable serial clock output, serial data output, transmission/reception, and interrupts and to clear the reception error flag.

UART/SIO serial status and data register (SSR0)

This register indicates the transmission/reception status and error status of UART/SIO.

• UART/SIO serial input data register (RDR0)

This register holds the receive data. The serial input is converted and then stored in this register.

UART/SIO serial output data register (TDR0)

This register sets the transmit data. Data written to this register is serial-converted and then outputted.

## ■ Input Clock

The UART/SIO uses the output clock (internal clock) from the dedicated baud rate generator or the input signal (external clock) from the UCK pin as its input clock (serial clock).
# 20.3 Channels of UART/SIO

## This section describes the channels of UART/SIO.

## Channels of UART/SIO

MB95130/M series contains 1 channel of UART/SIO. Table 20.3-1 and Table 20.3-2 shows the correspondence the channel, pin, and register.

#### Table 20.3-1 Pins of UART/SIO

Channel	Pin name	Pin function
	UCK0	Clock input/output
0	UO0	Data output
	UIO	Data input

#### Table 20.3-2 Registers of UART/SIO

Channel	Register name	Corresponding register (Name in this manual)
	SMC10	UART/SIO serial mode control register 1
	SMC20	UART/SIO serial mode control register 2
0	SSR0	UART/SIO serial status and data register
	TDR0	UART/SIO serial output data register
	RDR0	UART/SIO serial input data register

# 20.4 Pins of UART/SIO

## This section describes the pins related to the UART/SIO.

#### Pins Related to UART/SIO

The pins associated with UART/SIO are the clock input and output pin (UCK0), serial data output pin (UO0) and serial data input pin (UI).

#### UCK0:

Clock input/output pin for UART/SIO.

When the clock output is enabled (SMC20:SCKE=1), it serves as a UART/SIO clock output pin (UCK0) regardless of the value of the corresponding port direction register. At this time, do not select the external clock (set SMC10:CKS = 0).

When it is to be used as a UART/SIO clock input pin, disable the clock output (SMC20:SCKE = 0) and make sure that it is set as input port by the corresponding port direction register. At this time, be sure to select the external clock (set SMC10:CKS = 0).

#### UO0:

Serial data output pin for UART/SIO. When the serial data output is enabled (SMC20:TXOE = 1), it serves as a UART/SIO serial data output pin (UO0) regardless of the value of the corresponding port direction register.

#### UIO:

Serial data input pin for UART/SIO. When it is to be used as a UART/SIO serial data input pin, make sure that it is set as input port by the corresponding port direction register.

# ■ Block Diagram of Pins Related to UART/SIO



Figure 20.4-1 Block Diagram of Pins Related to UART/SIO (UI0, UO0, UCK0)

# 20.5 Registers of UART/SIO

The registers related to UART/SIO are UART/SIO serial mode control register 1 (SMC10), UART/SIO serial mode control register 2 (SMC20), UART/SIO serial status and data register (SSR0), UART/SIO serial output data register (TDR0), and UART/SIO serial input data register (RDR0).

## Registers Related to UART/SIO

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0056 <sub>H</sub> SMC10	BDS	PEN	TDP	SBL	CBL1	CBL0	CKS	MD	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
UART/SIO serial	mode cor	ntrol regi	ster 2 (S	MC20)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0057 <sub>H</sub> SMC20	SCKE	TXOE	RERC	RXE	TXE	RIE	TCIE	TEIE	00100000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
UART/SIO serial	status an	d data re	egister (S	SR0)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0058 <sub>H</sub> SSR0	-	-	PER	OVE	FER	RDRF	TCPL	TDRE	00000001 <sub>B</sub>
	R0/WX	R0/WX	R/WX	R/WX	R/WX	R/WX	R(RM1), W	R/WX	
UART/SIO serial	output da	ita regist	er (TDR(	))					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0059 <sub>H</sub> TDR0	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
UART/SIO serial	input data	a registe	r (RDR0)	)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
005A <sub>H</sub> RDR0				P/M/Y	R/WX	R/WX	R/WX	R/WX	
005A <sub>H</sub> RDR0	R/WX	R/WX	R/WX						
005A <sub>H</sub> RDR0 R0/WX: Un	R/WX	R/WX	value is '	'0", writir	ng has no	o effect o	n operat	ion)	
005A <sub>H</sub> RDR0 R0/WX: Un R/W: Re	R/WX defined bi adable/wr	R/WX it (Read v itable (R	value is ' ead valu	'0", writir e is the s	ng has no same as	o effect o write val	n operat ue)	ion)	
005A <sub>H</sub> RDR0 R0/WX: Un R/W: Re R(RM1), W: Re	R/WX defined bi adable/wr adable/wr	R/WX it (Read v itable (R itable (R	value is ' ead valu ead valu	'0", writir e is the s e is diffe	ng has no same as rent from	o effect o write val n write va	n operat ue) alue, "1" i	ion) is read by	read-modify-write
005A <sub>H</sub> RDR0 R0/WX: Un R/W: Re R(RM1), W: Re (RI	R/WX defined bi adable/wr adable/wr /W) instru	R/WX it (Read itable (R itable (R uction)	value is ' ead valu ead valu	'0", writir e is the s e is diffe	ng has no same as rent fron	o effect o write val n write va	n operat ue) alue, "1" i	ion) is read by	read-modify-write

Figure 20.5-1 Registers Related to UART/SIO

# 20.5.1 UART/SIO Serial Mode Control Register 1 (SMC10)

UART/SIO serial mode control register 1(SMC10) controls the UART/SIO operation mode. The register is used to set the serial data direction (endian), parity and its polarity, stop bit length, operation mode (synchronous/asynchronous), data length, and serial clock.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	
Address	BDS	PEN	TDP	SBI	CBI 1	CBL 0	CKS	MD	0000000	
0056H SMC10		-		- ODL		- DEC	-		00000000	
				R/W	R/W	R/W	R/W	R/W		
			ME	)		0	peration	mode s	election bit	
			→ 0	Clo	ck async	hronous	mode (l	JART)		
			1	Clo	ck synch	ronous r	node (S	IO)		
			—>Ска	6	Clock selection bit					
			0	Ded	Dedicated baud rate generator					
			1	Exte	External clock (cannot be used in clock asynchronous mode)					
				1 CBL0		Cha	racter b	it length	control bits	
			0	0	5 bits					
			0	1	6 bits					
			1	0	7 bits					
			1	1	8 DIts					
			→SBI	-		5	Stop bit I	ength co	ntrol bit	
			0	1-bit	t length					
			1	2-bi	length					
			→ TDF				Parit	y polarity	/ bit	
			0	Eve	n parity					
			1	Odd	parity					
				1			Parit	ty contro	bit	
			0	No p	arity					
			1	With	parity					
						Ser	ial data	direction	control bit	
			0	Tran	smit/rece	eive data	from LS	SB side s	sequentially	
			1	Tran	smit/rece	eive data	from M	SB side	sequentially	

	Bit name	Function							
bit7	BDS: Serial data direction control bit	This bit sets the serial data direction (endian).         Setting this bit to "0":       the bit specifies transmission or reception to be performed sequentially starting from the LSB side in the serial data register.         Setting this bit to "1":       the bit specifies transmission or reception to be performed sequentially starting from the MSB side in the serial data register.							
bit6	PEN: Parity control bit	This bit enables or disables parity in clock asynchronous mode. Setting this bit to "0": no parity Setting this bit to "1": with parity							
bit5	TDP: Parity polarity bit	This bit controls even/odd parity. Setting this bit to "0": specifies even parity Setting this bit to "1": specifies odd parity							
bit4	SBL: Stop bit length control bit	<ul> <li>This bit controls the length of the stop bit in clock asynchronous mode.</li> <li>Setting this bit to "0": sets the stop bit length to "1".</li> <li>Setting this bit to "1": sets the stop bit length to "2".</li> <li>Note: The setting of this bit is only valid for transmission operation in clock asynchronous mode. For receiving operation, reception data register full flag is se to "1" after detecting stop bit(1-bit) and completing the reception regardless of this bit.</li> </ul>							
bit3 bit2	CBL1, 0: Character bit length control bit	These bits select the character bit length as shown in the following table:CBL1CBL0Character bit length005016107118• The above setting is valid in both asynchronous and synchronous modes.							
bit1	CKS: Clock selection bit	This bit selects the external clock or dedicated baud rate generator. Setting the bit to "0" selects the dedicated baud rate generator. Setting the bit to "1" selects the external clock. Note: Setting this bit to "1" forcibly disables the output of the UCK pin. The external clock cannot be used in clock asynchronous mode (UART).							
bit0	MD: Operation mode selection bit	This bit selects clock asynchronous mode (UART) or clock synchronous mode (SIO). Setting the bit to "0" selects clock asynchronous mode (UART). Setting the bit to "1" selects clock synchronous mode (SIO).							

## Table 20.5-1 Functional Description of Each Bit of UART/SIO Serial Mode Control Register 1 (SMC10)

Note:

When modifying the UART/SIO serial mode control register 1 (SMC10), do not perform the modification during data transmission or reception.

# 20.5.2 UART/SIO Serial Mode Control Register 2 (SMC20)

UART/SIO serial mode control register 2 (SMC20) controls the UART/SIO operation mode. The register is used to enable/disable serial clock output, serial data output, transmission/reception, and interrupts and to clear the reception error flag.

# ■ UART/SIO Serial Mode Control Register 2 (SMC20)



	Bit name	Function
bit7	SCKE: Serial clock output enable bit	<ul> <li>This bit controls the input/output of the serial clock (UCK) pin in clock synchronous mode.</li> <li>Setting the bit to "0" allows the pin to be used as a general-purpose port.</li> <li>Setting the bit to "1" enables clock output.</li> <li>Note: When CKS is "1", the internal clock signal is not outputted even with this bit set to "1". If this bit is set to "1" with SCM1:MD set to "0" (asynchronous mode), the output from the port will always be "H".</li> </ul>
bit6	TXOE: Serial data output enable bit	This bit controls the output of the serial data (UO pin). Setting the bit to "0" allows the pin to be used as a general-purpose port. Setting the bit to "1" enables serial data output.
bit5	RERC: Reception error flag clear bit	Setting the bit to "0" clears the SSR register error flags (PER, OVE, FER). Setting the bit to "1" clears the reception error flag. Reading this bit always returns "1".
bit4	RXE: Reception operation enable bit	Setting the bit to "0" disables the reception of serial data.         Setting the bit to "1" enables the reception of serial data.         If this bit is set to "0" during reception, the reception operation will be immediately disabled and initialization will be performed. The data received up to that point will not be transferred to the UART/SIO serial input data register.         Note:       Setting this bit to "0" initializes reception operation. It has no effect on the interrupt flags (PER, OVE, FRE, RDRF).
bit3	TXE: Transmission operation enable bit	<b>Setting the bit to "0"</b> disables the transmission of serial data. <b>Setting the bit to "1"</b> enables the transmission of serial data. If this bit is set to "0" during transmission, the transmission operation will be immediately disabled and initialization will be performed. The transmission completion flag (TCPL) will be set to "1" and the transmission data register empty (TDRE) bit will also be set to "1".
bit2	RIE: Reception interrupt enable bit	Setting the bit to "0" disables reception interrupt. Setting the bit to "1" enables reception interrupt. A reception interrupt occurs immediately after either the receive data register full (RDRF) bit or an error flag (PER, OVE, FER, or RDRF) is set to "1" with this bit set to "1" (enabled).
bit1	TCIE: Transmission completion interrupt enable bit	Setting the bit to "0" disables interrupts by the transmission completion flag. Setting the bit to "1" enables interrupts by the transmission completion flag. A transmission interrupt occurs immediately after the transmission completion flag (TCPL) bit is set to "1" with this bit set to "1" (enabled).
bit0	TEIE: Transmission data register empty interrupt enable bit	Setting the bit to "0" disables interrupts by the transmission data register empty. Setting the bit to "1" enables interrupts by the transmission data register empty. A transmission interrupt occurs immediately after the transmission data register empty (TDRE) bit is set to "1" with this bit set to "1" (enabled).

# Table 20.5-2 Functional Description of Each Bit of UART/SIO Serial Mode Control Register 2 (SMC20)

# 20.5.3 UART/SIO Serial Status and Data Register (SSR0)

# The UART/SIO serial status and data register (SSR0) indicates the transmission/ reception status and error status of the UART/SIO.

# ■ UART/SIO Serial Status and Data Register (SSR0)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
Address	-	-	PER	OVE	FER	RDRF	TCPL	TDRE	0000001в
0058H SSR0					<u> </u>	<b>D A A O (</b>			
	R0/WX	R0/WX	R/WX	R/WX	R/WX	R/WX	R(RM1), W	R/WX	
			TDRE		Tr	ansmiss	ion data	register	empty flag
			0 Т	ransmit	data pre	esent			
		l	1   T	ransmit	data ab	sent			
			TCPL			Transm	ission c	ompletior	n flag
			0 0	Cleared b	by writin	g "0"			
		l	1 5	Serial tra	nsmissio	on comp	lete		
		>	RDRF			Recept	ion data	register	full flag
			0 R	Receive o	data abs	ent			
		L	1 R	Receive o	data pre	sent			
		>	FER			Fi	raming e	error flag	
			0 F	raming e	error ab	sent			
		l	1 F	raming e	error pre	esent			
		>	OVE			0	verrun e	error flag	
			0 0	Overrun e	error abs	sent			
		l	1 0	Overrun e	error pre	esent			
		>	PER			I	Parity er	ror flag	
			0 F	Parity err	or absei	nt			
		l	1   F	rarity err	or prese	ent			
R/W: Read	dable/writ	table (Re	ead valu	e is the	same as	s write va	alue)		
R0/WX: Unde R(RM1), W: Read	efined bit dable/writ	(Read v table (Re	/alue is ' ead valu	'0", writir e is diffe	ng has n rent fror	no ef fect m write v	: on ope /alue.	ration)	
"1" is	s read by	read-m	odify-wr	ite (RMV	V) instru	iction)			
K/VVX: Read	l value	eadable,	, writing	nas no e	ei tect of	operati	un)		

#### Figure 20.5-4 UART/SIO Serial Status and Data Register (SSR0)

	Bit name	Function
bit7 bit6	Unused bit	<ul><li>These bits are not used.</li><li>Reading always returns "0".</li><li>Writing to the bits has no effect on operation.</li></ul>
bit5	PER: Parity error flag	<ul> <li>This flag detects a parity error in receive data.</li> <li>The bit is set when a parity error occurs during reception. Writing "0" to the RERC bit clears this flag.</li> <li>If error detection and clearing by RERC occur at the same time, the error flag is set preferentially.</li> </ul>
bit4	OVE: Overrun error flag	<ul> <li>This flag detects an overrun error in receive data.</li> <li>The flag is set when an overrun error occurs during reception. Writing "0" to the RERC bit clears this flag.</li> <li>If error detection and clearing by RERC occur at the same time, the error flag is set preferentially.</li> </ul>
bit3	FER: Framing error flag	<ul> <li>This flag detects a framing error in receive data.</li> <li>The bit is set when a framing error occurs during reception. Writing "0" to the RERC bit clears this flag.</li> <li>If error detection and clearing by RERC occur at the same time, the error flag is set preferentially.</li> </ul>
bit2	RDRF: Receive data register full flag	<ul> <li>This flag indicates the status of the UART/SIO serial input data register.</li> <li>The bit is set to "1" when receive data is loaded to the serial input data register.</li> <li>The bit is cleared to "0" when data is read from the serial input data register.</li> </ul>
bit1	TCPL: Transmission completion flag	<ul> <li>This flag indicates the data transmission status.</li> <li>The bit is set to "1" upon completion of serial transmission. Note, however, that the bit is not set to "1" even upon completion of transmission when the UART/SIO serial output data register contains data to be transmitted in succession.</li> <li>Writing "0" to this bit clears its flag.</li> <li>If events to set and clear the flag occur at the same time, it is set preferentially.</li> <li>Writing "1" to this bit has no effect on operation.</li> </ul>
bit0	TDRE: Transmission data register empty flag	<ul> <li>This flag indicates the status of the UART/SIO serial output data register.</li> <li>The bit is set to "0" when transmit data is written to the serial output register.</li> <li>The bit is set to "1" when data is loaded to the transmission shift register and transmission starts.</li> </ul>

# Table 20.5-3 Functional Description of Each Bit of UART/SIO Serial Status and Data Register (SSR0)

# 20.5.4 UART/SIO Serial Input Data Register (RDR0)

# The UART/SIO serial input data register (RDR0) is used to input (receive) serial data.

# ■ UART/SIO Serial Input Data Register (RDR0)

Figure 20.5-5 shows the bit configuration of the UART/SIO serial input data register.

#### Figure 20.5-5 UART/SIO Serial Input Data Register (RDR0)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
005A <sub>H</sub> RDR0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	00000000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	
2/W/X: Read only	(Readab	le writin	a bas no	offect o	n oporati	on)			

This register stores received data. The serial data signals sent to the serial data input pin (UI0 pin) is converted by the shift register and stored in this register.

When received data is set correctly in this register, the receive data register full (RDRF) bit is set to "1". At this time, an interrupt occurs if reception interrupt requests have been enabled. If an RDRF bit check by the program or using an interruption shows that received data is stored in this register, the reading of the content for this register clears the RDRF flag to "0".

When the character bit length (CBL1, 0) is set to shorter than 8 bits, the excess upper bits (beyond the set bit length) are set to "0".

# 20.5.5 UART/SIO Serial Output Data Register (TDR0)

## The UART/SIO serial output data register (TDR0) is used to output (transmit) serial data.

## UART/SIO Serial Output Data Register (TDR0)

Figure 20.5-6 shows the bit configuration of the UART/SIO serial output data register.

	-							-	
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0059 <sub>H</sub> TDR0	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	00000000 <sub>B</sub>
	R/W								

#### Figure 20.5-6 UART/SIO Serial Output Data Register (TDR0)

This register holds data to be transmitted. The register accepts a write when the transmission data register empty (TDRE) bit contains "1". An attempt to write to the bit is ignored when the bit contains "0".

When this register is updated at writing complete the transmission data and TDRE=0 (without depending on TXE of the UART/SIO serial mode control register is "1" or "0"), the transmission operation is initialized by writing "0" to TXE, TDRE becomes "1", and the update of this register becomes possible. Moreover, when "0" is written in TXE without the starting transmission (when the transmission data is written in TDR, and it has not transmitted TXE to "1" yet), TCPL is not set in "1". The transmission data is transferred to the shift register for the transmission, it is converted into the serial data, and it is transmitted from the serial data output terminal.

When transmit data is written to the UART/SIO serial output data register (TDR0), the transmission data register empty bit (TDRE) is set to "0". Upon completion of transfer of transmit data to the transmission shift register, the transmission data register empty bit (TDRE) is set to "1", allowing the next piece of transmit data to be written. At this time, an interrupt occurs if transmission data register empty interrupts have been enabled. Write the next piece of transmit data when transmit data empty occurs or the transmit data empty (TDRE) bit is set to "1".

When the character bit length (CBL1, 0) is set to shorter than 8 bits, the excess upper bits (beyond the set bit length) are ignored.

#### Note:

The data in this register cannot be updated when TDRE in UART/SIO serial status data register is "0".

When this register is updated at writing complete the transmission data and TDRE=0 (without depending on TXE of the UART/SIO serial mode control register 2 is "1" or "0"), the transmission operation is initialized by writing "0" to TXE, TDRE becomes "1", and the update of this register becomes possible.

Moreover, when "0" is written in TXE without the starting transmission (when the transmission data is written in TDR, and it has not transmitted TXE to "1" yet), TCPL is not set in "1". And, to change data, please write it after making TDRE "1" once by writing TXE =0.

# 20.6 Interrupts of UART/SIO

# The UART/SIO has six interrupt-related bits: error flag bits (PER, OVE, FER), receive data register full bit (RDRF), transmission data register empty bit (TDRE), and transmission completion flag (TCPL).

## Interrupts of UART/SIO

Table 20.6-1 lists the UART/SIO interrupt control bits and interrupt sources.

Table 20.6-1 UART/SIO Interrupt Control Bits and Interrupt Sources

Item	Description							
Interrupt request flag bit	SSR: TDRE	SSR: TCPL	SSR: RDRF	SSR: PER	SSR: OVE	SSR: FER		
Interrupt request enable bit	SMC2: TEIE	SMC2: TCIE	SMC2: RIE	SMC2: RIE	SMC2: RIE	SMC2: RIE		
Interrupt source	Transmission data register empty	Transmission completion	Receive data full	Parity error	Overrun error	Framing error		

## Transmission Interrupt

When transmit data is written to the UART/SIO serial output data register (TDR), the data is transferred to the transmission shift register. When the next piece of data can be written, the TDRE bit is set to "1". At this time, an interrupt request to the interrupt controller occurs when transmit data register empty interrupt enable bit has been enabled (SMC2:TEIE = 1).

The TCPL bit is set to "1" upon completion of transmission of all pieces of transmit data. At this time, an interrupt request to the interrupt controller occurs when transmission completion interrupt enable bit has been enabled (SMC2:TCIE = 1).

## Reception Interrupt

If the data is inputted successfully up to the stop bit, the RDRF bit is set to 1. If an overrun, parity, or framing error occurs, the corresponding error flag bit (PER, OVE, or FER) is set to "1".

These bits are set when a stop bit is detected. If reception interrupt enable bit has been enabled (SMC2:RIE = 1), an interrupt request to the interrupt controller will be generated.

Refer to "CHAPTER 8 INTERRUPTS" for the interrupt request numbers and vector tables of all peripheral functions.

## Registers and Vector Table Related to UART/SIO Interrupts

#### Table 20.6-2 Registers and Vector Table Related to UART/SIO Interrupts

Interrupt	pt Interrupt	Interrupt level	setting register	Vector table address		
source	request No.	Register	Setting bit	Upper	Lower	
ch.0	IRQ4	ILR1	L04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	

ch.: channel

# 20.7 Explanation of UART/SIO Operations and Setup Procedure Example

The UART/SIO has a serial communication function (operation mode 0, 1).

# Operation of UART/SIO

• Operation mode

Two operation modes are available in the UART/SIO. Clock synchronous mode (SIO) or clock asynchronous mode (SUAR) can be selected (see Table 20.7-1).

Table 20.7-1 Operation Modes of UART/SIO

Operation mode	Data	a length	Synchronization	l ength of stop bit		
Operation mode	No parity With parity		mode	Length of stop bit		
	5	6				
0	6	7	Asynchronous	1 bit or 2 bits		
0	7	8	Asynchronous			
	8	9				
	5	-				
1	6	-	Synchronous			
	7	-	Synchronous	-		
	8	-				

## Setup Procedure Example

The UART/SIO is set up in the following procedure.

- Initial setup
  - 1) Set the port input. (DDR1)
  - 2) Set the interrupt level. (ILR1)
  - 3) Set the prescaler. (PSSR)
  - 4) Set the baud rate. (BRSR)
  - 5) Select the clock. (SMC10:CKS)
  - 6) Set the operation mode. (SMC10:MD)
  - 7) Enable/disable the serial clock output. (SMC20:SCKE)
  - 8) Enable reception. (SMC20:RXE = 1)
  - 9) Enable interrupts. (SMC20:RIE = 1)
- Interrupt processing

Read receive data. (RDR0)

# 20.7.1 Operating Description of Operation Mode 0

## Operation mode 0 operates as clock asynchronous mode (UART).

## Operating Description of UART/SIO Operation Mode 0

Clock asynchronous mode (UART) is selected when the MD bit in the UART/SIO serial mode control register 1 (SMC10) is set to "0".

#### Baud rate

The serial clock is selected by the CKS bit in the SMC10 register. Be sure to select the dedicated baud rate generator at this time.

The baud rate is equivalent to the output clock frequency of the dedicated baud rate generator, divided by four. The UART can perform communication within the range from -2% to +2% of the selected baud rate.

The baud rate generated by the dedicated baud rate generator is obtained from the equation illustrated below. (For information about the dedicated baud rate generator, refer to "CHAPTER 21 UART/SIO DEDICATED BAUD RATE GENERATOR".)





# Table 20.7-2 Sample Asynchronous Transfer Rates Based on Dedicated Baud Rate Generator (Clock Gear = 4/F<sub>CH</sub>, Machine Clock = 10MHz, 16MHz, 16.25MHz)

Dedicated baud rat	e generator setting	Internal	Total division natio	Baud rate	Baud rate	Baud rate	
Prescaler selection PSS[1:0]	Baud rate counter setting BRS[7:0]	UART division	(PSS x BRS x 4)	(10MHz / Total division ratio)	(16MHz / Total division ratio)	Total division ratio)	
1 (Setting value: 0,0)	20	4	80	125000	200000	203125	
1 (Setting value: 0,0)	22	4	88	113636	181818	184659	
1 (Setting value: 0,0)	44	4	176	56818	90909	92330	
1 (Setting value: 0,0)	87	4	348	28736	45977	46695	
1 (Setting value: 0,0)	130	4	520	19231	30769	31250	
2 (Setting value: 0,1)	130	4	1040	9615	15385	15625	
4 (Setting value: 1,0)	130	4	2080	4808	7692	7813	
8 (Setting value: 1,1)	130	4	4160	2404	3846	3906	

The baud rate in clock asynchronous mode can be set in the following range.

PSS[1:0]	BRS[7:0]
$00_{\rm B}$ to $11_{\rm B}$	$02_{\rm H}(2)$ to FF <sub>H</sub> (255)

# Table 20.7-3 Baud Rate Setting Range in Clock Asynchronous Mode

#### Transfer data format

UART can treat data only in NRZ (Non-Return-to-Zero) format. Figure 20.7-2 shows the data format.

The character bit length can be selected from among 5 to 8 bits depending on the CBL1 and CBL0 settings.

The stop bit length can be set to 1 or 2 bits depending on the SBL setting.

PEN and TDP can be used to enable/disable parity and to select parity polarity.

As shown in Figure 20.7-2, the transfer data always starts from the start bit ("L" level) and ends with the stop bit ("H" level) by performing the specified data bit length transfer with MSB first or LSB first ("LSB first" or "MSB first" can be selected by the BDS bit). It becomes "H" level at the idle state.

Figure 20.7-2 Transfer Data Format



#### Receiving operation in asynchronous clock mode (UART)

Use UART/SIO serial mode control register 1 (SMC10) to select the serial data direction (endian), parity/ non-parity, parity polarity, stop bit length, character bit length, and clock.

Reception remains performed as long as the reception operation enable bit (RXE) contains "1".

Upon detection of a start bit in receive data with the reception operation enable bit (RXE) set to "1", one frame of data is received according to the data format set in UART/SIO serial control register 1 (SMC10).

When the reception of one frame of data has been completed, the received data is transferred to the UART/ SIO serial input data register (RDR0) and the next frame of serial data can be received.

When the UART/SIO serial input data register (RDR0) stores data, the receive data register full (RDRF) bit is set to "1".

A reception interrupt occurs the moment the receive data register full (RDRF) bit is set to "1" when the reception interrupt enable bit (RIE) contains "1".

Received data is read from the UART/SIO serial input data register (RDR0) after each error flag (PER, OVE, FER) in the UART/SIO serial status and data register is checked.

When received data is read from the UART/SIO serial input data register (RDR0), the receive data register full (RDRF) bit is cleared to "0".

Note that modifying UART/SIO serial mode control register 1 (SMC10) during reception may result in unpredictable operation. If the RXE bit is set to "0" during reception, the reception is immediately disabled and initialization will be performed. The data received up to that point will not be transferred to the serial input data register.

RXE _	
UI	St D0 D1 D2 D3 D4 D5 D6 D7 Sp Sp St D0 D1 D2
RDR0 read —	
RDRF_	

Figure 20.7-3 Receiving Operation in Asynchronous Clock Mode

Reception error in asynchronous clock mode (UART)

If any of the following three error flags (PER, FER, OVE) has been set, receive data is not transferred to the UART/SIO serial input data register (RDR0) and the receive data register full (RDRF) bit is not set to "1" either.

• Parity error (PER)

The parity error (PER) bit is set to "1" if the parity bit in received serial data does not match the parity polarity bit (TDP) when the parity control bit (PEN) contains "1".

• Framing error (FER)

The framing error (FER) bit is set to "1" if "1" is not detected at the position of the first stop bit in serial data received in the set character bit length (CBL) under parity control (PEN). Note that the stop bit is not checked if it appears at the second bit or later.

• Overrun error (OVE)

Upon completion of reception of serial data, the overrun error (OVE) bit is set to "1" if the reception of the next data is performed before the previous receive data is read.

Each flag is set at the position of the first stop bit.



#### Figure 20.7-4 Setting Timing for Receiving Errors

#### Start bit detection and confirmation of receive data during reception

The start bit is detected by a falling of the serial input followed by a succession of three "L" levels after the serial data input is sampled according to the clock (BRCLK) signal provided by the dedicated baud rate generator with the reception operation enable bit (RXE) set to "1". When the first "H", "L", "L", "L", "L" train is detected in a BRCLK sample, therefore, the current bit is regarded as the start bit.

The frequency-quartered circuit is activated upon detection of the start bit and serial data is inputted to the reception shift register at intervals of four periods of BRCLK.

When data is received, sampling is performed at three points of the baud rate clock (BRCLK) and data sampling clock (DSCLK) and received data is confirmed on a majority basis when two bits out of three match.



Figure 20.7-5 Start Bit Detection and Serial Data Input

#### Transmission in asynchronous clock mode

Use UART/SIO serial mode control register 1 (SMC10) to select the serial data direction (endian), parity/ non-parity, parity polarity, stop bit length, character bit length, and clock.

Either of the following two procedures can be used to initiate the transmission process:

- Set the transmission operation enable bit (TXE) to "1", and then write transmit data to the serial output data register to start transmission.
- Write transmit data to the UART/SIO serial output data register, and then set the transmission operation enable bit (TXE) to "1" to start transmission.

Transmit data is written to the UART/SIO serial output data register (TDR0) after it is checked that the transmit data register empty (TDRE) bit set to "1".

When the transmit data is written to the UART/SIO serial output data register (TDR0), the transmit data register empty (TDRE) bit is cleared to "0".

The transmit data is transferred from the UART/SIO serial output data register (TDR0) to the transmission shift register, and the transmit data register empty (TDRE) is set to "1".

When the transmission interrupt enable bit (TIE) contains "1", a transmission interrupt occurs if the transmit data register empty (TDRE) bit is set to "1". This allows the next piece of transmit data to be written to the UART/SIO serial output data register (TDR0) by interrupt handling.

To detect the completion of serial transmission by transmission interrupt, set the transmission completion interrupt enable bits as follows: TEIE = 0, TCIE = 1. Upon completion of transmission, the transmission completion flag (TCPL) is set to "1" and a transmission interrupt occurs.

Both the transmission completion flag (TCPL) and the transmission data register empty flag (TDRE), when transmitting data consecutively, are set at the position which the transmission of the last bit was completed (it varies depending on the data length, parity enable, or stop bit length setting), as shown in Figure 20.7-6 below.

Note that modifying UART/SIO serial mode control register 1 (SMC10) during transmission may result in unpredictable operation.



Figure 20.7-6 Transmission in Asynchronous Clock Mode (UART)

The TDRE flag is set at the point indicated in the following figure if the preceding piece of transmit data does not exist in the transmission shift register.





Figure 20.7-8 Setting Timing 2 for Transmit Data Register Empty Flag (TDRE) (When TXE Is Switched from "0" to "1")



#### Concurrent transmission and reception

In asynchronous clock mode (UART), transmission and reception can be performed independently. Therefore, transmission and reception can be performed at the same time or even with transmitting and receiving frames overlapping each other in shifted phases.

# 20.7.2 Operating Description of Operation Mode 1

## Operation mode 1 operates in synchronous clock mode.

## Operating Description of UART/SIO Operation Mode 1

Setting the MD bit in UART/SIO serial mode control register 1 (SMC10) to "1" selects synchronous clock mode (SIO).

The character bit length in synchronous clock mode (SIO) is variable between 5 bits and 8 bits.

Note, however, that parity is disabled and no stop bit is used.

The serial clock is selected by the CKS bit in the SMC10 register. Select the dedicated baud rate generator or external clock. The SIO performs shift operation using the selected serial clock as a shift clock.

To input the external clock signal, set the SCKE bit to "0".

To output the dedicated baud rate generator output as a shift clock signal, set the SCKE bit to "1". The serial clock signal is obtained by dividing clock by two, which is supplied by the dedicated baud rate generator. The baud rate in the SIO mode can be set in the following range. (For more information about the dedicated baud rate generator, also refer to "CHAPTER 21 UART/SIO DEDICATED BAUD RATE GENERATOR")

#### Table 20.7-4 Baud Rate Setting Range in SIO Mode

PSS[1:0]	BRS[7:0]			
$00_{\rm B}$ to $11_{\rm B}$	$01_{\rm H}(1)$ to FF <sub>H</sub> (255), $00_{\rm H}(256)$ (The highest and lowest baud rate settings are $01_{\rm H}$ and $00_{\rm H}$ , respectively.)			

The baud rate applied when the external clock or dedicated baud rate generator is used is obtained from the corresponding equation illustrated below.





		Machin	e clock (MCLK)		[bpo]
Baud rate value =	Г				[bps]
2.		1		1	
۷.	¢	2 4	×	256	
		8			
UART prescaler selection re Prescaler selection (PSS1, F	UART prescaler selection register (PSSR0) Prescaler selection (PSS1, PSS0)				g register (BRSR0) S7 to BRS0)

#### Figure 20.7-10 Baud Rate Calculation Formula for Using Dedicated Baud Rate Generator

#### Serial clock

The serial clock signal is outputted under control of the output for transmit data. When only reception is performed, therefore, set transmission control (TXE = 1) to write dummy transmit data to the UART/SIO serial output register. Refer to the data sheet for the UCK clock value.

#### Reception in UART/SIO operation mode 1

For reception in operation mode 1, each register is used as follows.

SMC10 (UART/SI	O serial r	node con	trol regist	er 1)					
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	BDS	PEN	TDP	SBL	CBL1	CBL0	CKS	MD	SMC10
	0	×	×	×	0	0	0	1	
SMC20 (UART/SIC	) serial m	node cont	rol registe	er 2)					
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	SCKE	TXOE	RERC	RXE	TXE	RIE	TCIE	TEIE	SMC20
	0	0	0	0	0	0	×	×	
SSR0 (UART/SIO	serial sta	tus and d	lata regist	er)					
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	-	-	PER	OVE	FER	RDRF	TCPL	TDRE	SSR0
	×	×	×	0	×	0	×	×	
TDR0 (UART/SIO	serial out	put data	register)						
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	TDR0
	×	×	×	×	×	×	×	×	
RDR0 (UART/SIO	serial inp	out data re	egister)						
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	RDR0
	0	۲	0	0	0	0	0	0	
<ul> <li>⊚: Used bit</li> <li>x : Unused bit</li> <li>1 : Set "1"</li> <li>0 : Set "0"</li> </ul>									

#### Figure 20.7-11 Registers Used for Reception in Operation Mode 1

The reception depends on whether the serial clock has been set to external or internal clock.

#### <When external clock is enabled>

When the reception operation enable bit (RXE) contains "1", serial data is received always at the rising edge of the external clock signal.

#### <When internal clock is enabled>

The serial clock signal is outputted in accordance with transmission. Therefore, transmission must be performed even when only performing reception. The following two procedures can be used.

• Set the transmission operation enable bit (TXE) to "1", then write transmit data to the UART/SIO serial output data register to generate the serial clock signal and start reception.

• Write transmit data to the UART/SIO serial output data register, then set the transmission operation enable bit (TXE) to "1" to generate the serial clock signal and start reception.

When 5-bit to 8-bit serial data is received by the reception shift register, the received data is transferred to the UART/SIO serial input data register (RDR0) and the next piece of serial data can be received.

When the serial input data register stores data, the receive data register full (RDRF) bit is set to "1".

A reception interrupt occurs the moment the receive data register full (RDRF) bit is set to "1" when the reception interrupt enable bit (RIE) contains "1".

To read received data, read it from the UART/SIO serial input data register after checking the error flag (OVE) in the UART/SIO serial status and data register.

When received data is read from the UART/SIO serial input data register (RDR0), the receive data register full (RDRF) bit is cleared to "0".

UCK	
UI	D0 D1 D2 D3 D4 D5 D6 D7
Read to RDR0	
RDRF	
	Interrupt to interrupt controller

#### Figure 20.7-12 8-bit Reception of Synchronous CLK Mode

#### Operation when reception error occurs

When an overrun error (OVE) exists, received data is not transferred to the UART/SIO serial input data register (RDR0).

#### **Overrun error (OVE)**

Upon completion of reception for serial data, the overrun error (OVE) bit is set to "1" if the receive data register full (RDRF) bit has been set to "1" by the reception for the preceding piece of data.

UCK				
UI _	D0 D1 D6 D7	D0 D1 D6 D7	D0 D1 D6 D7	
Read to RDR0 -			Γ	
RDRF _				
OVE				

#### Transmission in UART/SIO operation mode 1

For transmission in operation mode 1, each register is used as follows.

Figur	e 20.7-1	3 Regi	sters Us	ed for	Transmi	ssion in	Operat	ion Mod	le 1
SMC10 (UART/SIO serial mode control register 1)									
,	bit7	bit6	bit5	, bit4	bit3	bit2	bit1	bit0	
	BDS	PEN	TDP	SBL	CBL1	CBL0	CKS	MD	SMC10
·	0	×	×	×	0	0	0	1	
SMC20 (UART/SIC	) serial m	ode cont	trol registe	ər 2)					
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	SCKE	TXOE	RERC	RXE	TXE	RIE	TCIE	TEIE	SMC20
	0	0	0	0	0	0	×	×	
SSR0 (UART/SIO s	serial stat	tus and d	lata regist	ier)					
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	-	-	PER	OVE	FER	RDRF	TCPL	TDRE	SSR0
	×	×	×	0	×	0	×	×	
TDR0 (UART/SIO	serial out	put data	register)						
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	TDR0
	×	×	×	×	×	×	×	×	
RDR0 (UART/SIO serial input data register)									
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	RDR0
	0	0	0	0	0	0	0	0	
<ul> <li>⊙ : Used bit</li> <li>x : Unused bit</li> <li>1 : Set "1"</li> </ul>									

The following two procedures can be used to initiate the transmission process:

- Set the transmission operation enable bit (TXE) to "1", then write transmit data to the UART/SIO serial output data register to start transmission.
- Write transmit data to the UART/SIO serial output data register, then set the transmission operation enable bit (TXE) to "1" to start transmission.

Transmit data is written to the UART/SIO serial output data register (TDR0) after it is checked that the transmit data register empty (TDRE) bit is set to "1".

When the transmit data is written to the UART/SIO serial output data register (TDR0), the transmit data register empty (TDRE) bit is cleared to "0".

When serial transmission is started after transmit data is transferred from the UART/SIO serial output data register (TDR0) to the transmission shift register, the transmit data register empty (TDRE) bit is set to "1".

When the use of the external clock signal has been set, serial data transmission starts at the fall of the first serial clock signal after the transmission process is started.

A transmission completion interrupt occurs the moment the transmit data register empty (TDRE) bit is set to "1" when the transmission interrupt enable bit (TIE) contains "1". At this time, the next piece of transmit data can be written to the UART/SIO serial output data register (TDR0). Serial transmission can be continued with the transmission operation enable bit (TXE) set to "1".

To use a transmission completion interrupt to detect the completion of serial transmission, enable transmission completion interrupt output this way: TEIE = 0, TCIE = 1. Upon completion of transmission, the transmission completion flag (TCPL) is set to "1" and a transmission completion interrupt occurs.



Figure 20.7-14 8-bit Transmission in Synchronous CLK Mode

Concurrent transmission and reception

<When external clock is enabled>

Transmission and reception can be performed independently of each other. Transmission and reception can therefore be performed at the same time or even when their phases are shifted from each other and overlapping.

<When internal clock is enabled>

As the transmitting side generates a serial clock, reception is influenced.

If transmission stops during reception, the receiving side is suspended. It resumes reception when the transmitting side is restarted.

 Refer to "20.4 Pins of UART/SIO" for operation with serial clock output and operation with serial clock input.

# 20.8 Sample Programs for UART/SIO

# We provide sample programs that can be used to operate UART/SIO.

## ■ Sample Programs for UART/SIO

For information about the sample programs for UART/SIO, refer to " Sample Programs" in Preface.

#### Setup Methods without Sample Program

• How to select the operation mode

The operation mode selection bit (SMC10:MOD) is used.

	Operation mode	Operation mode selection (MOD)
Mode 0	Asynchronous clock mode (UART)	Set the bit to "0"
Mode 1	Synchronous clock mode (SIO)	Set the bit to "1"

#### Operating clock types and selection method

The clock selection bit (SMC10:CKS) is used.

Clock input	Clock selection (CKS)
When selecting dedicated baud rate generator	Set the bit to "0"
When selecting external clock	Set the bit to "1"

How to use the UCK0, UI0, or UO0 pin

The following setting is used.

	UART	
When setting UCK0 pin as an input	DDR1:P12 = 0 SMC20:SCKE = 0	
When setting UCK0 pin as an output	SMC20:SCKE = 1	
When using UI0 pin	DDR1:P10 = 0	
When using UO0 pin	SMC20:TXOE = 1	

#### • How to enable/stop UART operation

The reception operation enable bit (SMC20:RXE) is used.

What is controlled	Reception operation enable bit (RXE)	
Disabling (stopping) reception	Set the bit to "0"	
Enabling reception	Set the bit to "1"	

The transmission operation control bit (SMC20:TXE) is used.

What is controlled	Transmission operation control bit (TXE)	
Disabling (stopping) transmission	Set the bit to "0"	
Enabling transmission	Set the bit to "1"	

#### • How to set parity

The parity control (SMC10:PEN) and parity polarity (SMC10:TDP) bits are used.

Operation	Parity control (PEN)	Parity polarity (TDP)
When selecting no parity	Set the bit to "0"	-
When selecting even parity	Set the bit to "1"	Set the bit to "0"
When selecting odd parity	Set the bit to "1"	Set the bit to "1"

#### • How to set the data length

The data length selection bit (SMC10:CBL[1:0]) is used.

Operation	Data length selection bit (CBL[1:0])	
When selecting 5-bit length	Specify "00 <sub>B</sub> "	
When selecting 6-bit length	Specify "01 <sub>B</sub> "	
When selecting 7-bit length	Specify "10 <sub>B</sub> "	
When selecting 8-bit length	Specify "11 <sub>B</sub> "	

• How to select the STOP bit length

The STOP bit length control bit (SMC10:SBL) is used.

Operation	STOP bit length control (SBL)	
When setting STOP bit to 1-bit length	Set SBL to "0"	
When setting STOP bit to 2-bit length	Set SBL to "1"	

#### How to clear error flags

The reception error flag clear bit (SMC20:RERC) is used.

What is controlled	Reception error flag clear bit (RERC)
When clearing error flags (PER, OVE, FER)	Write "0"

#### How to set the transfer direction

The serial data direction control bit (SMC10:BDS) is used.

LSB first or MSB first can be selected for the transfer direction in any operation mode.

What is controlled	Serial data direction control (BDS)	
When selecting LSB first transfer (from least significant bit)	Set the bit to "0"	
When selecting MSB first transfer (from most significant bit)	Set the bit to "1"	

How to clear the reception completion flag

The following setup is performed.

What is controlled	Method	
When clearing reception completion flag	Read from RDR0 register	

When the first read from the RDR0 register is performed, reception starts.

#### How to clear the transmission buffer empty flag

The following setup is performed.

What is controlled	Method	
When clearing transmission buffer empty flag	Write to TDR0 register	

When the first write to TDR0 register is performed, transmission starts.

#### How to set the baud rate

Refer to "20.7.1 Operating Description of Operation Mode 0".

#### Interrupt-related registers

The interrupt level setting registers shown in the following table are used to set the interrupt level.

	Interrupt level setting register	Interrupt vector
ch.0	Interrupt level register(ILR1) Address: 0007A <sub>H</sub>	#4 Address: 0FFF2 <sub>H</sub>

• How to enable/disable/clear interrupts

The interrupt request enable bits (SMC20:RIE, SMC20:TCIE, SMC20:TEIE) are used to enable interrupts.

	UART reception UART transmission		nsmission
	Reception interrupt enable bit (RIE)	Transmission completion interrupt enable bit (TCIE)	Transmission data register empty interrupt enable bit (TEIE)
When disabling interrupt requests	Select "0"		
When enabling interrupt requests	Select "1"		

Interrupt requests are cleared in the following setup procedure.

	UART reception	UART transmission
When clearing interrupt requests	Read from UART/SIO serial input register (RDR0) to clear reception data register full bit (RDRF).	Write data to UART/SIO serial output data register (TDR0) to
	Write "0" to error flag clear bit (RERC) to clear error flags (PER, OVE, FER) to "0".	empty bit (TDRE) to "0".

#### CHAPTER 20 UART/SIO

# CHAPTER 21 UART/SIO DEDICATED BAUD RATE GENERATOR

This chapter describes the functions and operations of the dedicated baud rate generator of UART/SIO.

- 21.1 Overview of UART/SIO Dedicated Baud Rate Generator
- 21.2 Channels of UART/SIO Dedicated Baud Rate Generator
- 21.3 Registers of UART/SIO Dedicated Baud Rate Generator
- 21.4 Operating Description of UART/SIO Dedicated Baud Rate Generator

# 21.1 Overview of UART/SIO Dedicated Baud Rate Generator

The UART/SIO dedicated baud rate generator generates the baud rate for the UART/SIO. The generator consists of the UART/SIO dedicated baud rate generator prescaler selection register (PSSR) and UART/SIO dedicated baud rate generator baud rate setting register (BRSR).

# ■ Block Diagram of UART/SIO Dedicated Baud Rate Generator





# Input Clock

The UART/SIO dedicated baud rate generator uses the output clock from the prescaler or the machine clock as its input clock.

# Output Clock

The UART/SIO dedicated baud rate generator supplies its clock to the UART/SIO.

# 21.2 Channels of UART/SIO Dedicated Baud Rate Generator

# This section describes the channels of the UART/SIO dedicated baud rate generator.

## ■ Channels of UART/SIO Dedicated Baud Rate Generator

MB95130/M series contains 1 channel of the UART/SIO dedicated baud rate generator.

Table 21.2-1 shows the correspondence the channel and registers.

#### Table 21.2-1 Registers of Dedicated Baud Rate Generator

Channel	Register name	Corresponding register (Name in this manual)
0	PSSR0	UART/SIO dedicated baud rate generator prescaler selection register
	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register

# 21.3 Registers of UART/SIO Dedicated Baud Rate Generator

The registers related to the UART/SIO dedicated baud rate generator are namely the UART/SIO dedicated baud rate generator prescaler selection register (PSSR) and UART/SIO dedicated baud rate generator baud rate setting register (BRSR).

## ■ Registers Related to UART/SIO Dedicated Baud Rate Generator

0FBE <sub>H</sub> PSSR0	-	-	-	-	-	BRGE	PSS1	PSS0	00000000 <sub>B</sub>
11	R0/WX	R0/WX	R0/WX	R0/WX	R0/WX	R/W	R/W	R/W	
UART/SIO dedica	ted baud bit7	rate ger	herator b	aud rate bit4	setting r	egister (l bit2	BRSR) bit1	bit0	Initial value
0FBF <sub>H</sub> BRSR0	BRS7	BRS6	BRS5	BRS4	BRS3	BRS2	BRS1	BRS0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
R0/WX : Undefine	ed bit (Re	ad value	e is "0", v	vriting ha	as no effe	ect on op	eration)		

#### Figure 21.3-1 Registers Related to UART/SIO Dedicated Baud Rate Generator
# 21.3.1 UART/SIO Dedicated Baud Rate Generator Prescaler Selection Register (PSSR)

The UART/SIO dedicated baud rate generator prescaler register (PSSR) controls the output of the baud rate clock and the prescaler.

### ■ UART/SIO Dedicated Baud Rate Generator Prescaler Selection Register (PSSR)

PSSR0	bit7 bit6	bit5 bit4	bit3 bit2	bit1 bit0	Initial value	
0FB	E <sub>H</sub>		- BRGE	PSS1 PSS0	0000000в	
	R0/WX R0/WXF	R0/WX R0/W>	K RO/WX R/W	R/W R/W		
	F	PSS1 PSS0	Preso	caler selection bits	6	
		0 0	1/1			
		0 1	1/2			
		1 0	1/4			
	L	1 1	1/8			
	_					
	└───→B	RGE	Baud rate	clock output enab	le bit	
		0 Disable	es baud rate outp	ut		
	L	1 Enable	baud rate outpu	t		
<ul> <li>R/W: Readable/writable (Read value is the same as write value)</li> <li>R0/WX: Undefined bit (Read value is "0", writing has no ef fect on operation)</li> <li>Initial value</li> </ul>						

### Figure 21.3-2 UART/SIO Dedicated Baud Rate Generator Prescaler Selection Register (PSSR)

Table 21.3-1 UART/SIO Dedicated Baud Rate Generator Prescaler Selection Register (PSSR)

Bit name	Function					
Unused bit	These bits are	not used. Rea	ding the bits always returns "0".			
BRGE: Baud rate clock output enable bit	This bit enables the output of the baud rate clock "BRCLK". <b>Setting the bit to ''1''</b> loads BRS[7:0] to the 8-bit down-counter and outputs "BRCLK", which is supplied to the UART/SIO. <b>Setting the bit to ''0''</b> stops the output of "BRCLK".					
PSS1, PSS0: Prescaler selection bit	PSS1	PSS0	Prescaler selection			
	0	0	1/1			
	0	1	1/2			
	1	0	1/4			
	1	1	1/8	]		
E E E E E E E E E E E E E E E E E E E	Bit name Jnused bit BRGE: Baud rate clock output nable bit PSS1, PSS0: Prescaler selection bit	Bit name     These bits are       Jnused bit     These bits are       BRGE:     This bit enable       Baud rate clock output     Setting the bi       nable bit     Setting the bi       PSS1, PSS0:     0       Prescaler selection bit     1	Bit name       These bits are not used. Rea         Jnused bit       These bits are not used. Rea         BRGE:       This bit enables the output of Setting the bit to "1" loads supplied to the UART/SIO. Setting the bit to "0" stops         PSS1, PSS0:       PSS1       PSS0         0       0       1         1       0       1         1       1       1	Bit name       Function         Jnused bit       These bits are not used. Reading the bits always returns "0".         BRGE:       This bit enables the output of the baud rate clock "BRCLK".         Setting the bit to "1" loads BRS[7:0] to the 8-bit down-consupplied to the UART/SIO.         Setting the bit to "0" stops the output of "BRCLK".         PSS1       PSS0         Prescaler selection         0       0         1       1/2         1       1/4         1       1/4         1       1/8		

### 21.3.2 UART/SIO Dedicated Baud Rate Generator Baud Rate Setting Register (BRSR)

The UART/SIO dedicated baud rate generator dedicated baud rate generator baud rate setting register (BRSR) controls the baud rate settings.

### ■ UART/SIO Dedicated Baud Rate Generator Baud Rate Setting Register (BRSR)

Figure 21.3-3 UART/SIO Dedicated Baud Rate Generator Baud Rate Setting Register (BRSR)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FBF <sub>H</sub> BRSR0	BRS7	BRS6	BRS5	BRS4	BRS3	BRS2	BRS1	BRS0	00000000 <sub>B</sub>
	R/W								

R/W: Readable/writable (Read value is the same as write value)

This register sets the cycle of the 8-bit down-counter and can be used to set any baud rate clock. Write to the register when the UART is stopped.

Do not set BRS[7:0] to " $00_H$ " or " $01_H$ " in clock asynchronous mode.

### 21.4 Operating Description of UART/SIO Dedicated Baud Rate Generator

## The UART/SIO dedicated baud rate generator serves as the baud rate generator for asynchronous clock mode.

### Baud Rate Setting

The SMC10 register (CKS bit) of the UART/SIO is used to select the serial clock. This selects the UART/SIO dedicated baud rate generator.

In asynchronous CLK mode, the shift clock that is selected by the CKS bit and divided by four is used and transfers can be performed within the range from -2% to +2%. The baud rate calculation formula for the UART/SIO dedicated baud rate generator is shown below.

### Figure 21.4-1 Baud Rate Calculation Formula when UART/SIO Dedicated Baud Rate Generator Is Used



## Table 21.4-1Sample Asynchronous Transfer Rates by Baud Rate Generator (Machine Clock = 10MHz, 16MHz, 16.25MHz)

UART/SIO Dedicated set	d baud rate generator ting	UART	Total division	Baud rate	Baud rate (16MHz /	Baud rate (16.25MHz /	
Prescaler selection PSS[1:0]	Baud rate counter setting BRS [7:0]	division	(PSS x BRS x4)	division ratio)	Total division ratio)	Total division ratio)	
1 (Setting value: 0, 0)	20	4	80	125000	200000	203125	
1 (Setting value: 0, 0)	22	4	88	113636	181818	184659	
1 (Setting value: 0, 0)	44	4	176	56818	90909	92330	
1 (Setting value: 0, 0)	87	4	348	28736	45977	46695	
1 (Setting value: 0, 0)	130	4	520	19231	30769	31250	
2 (Setting value: 0, 1)	130	4	1040	9615	15385	15625	
4 (Setting value: 1, 0)	130	4	2080	4808	7692	7813	
8 (Setting value: 1, 1)	130	4	4160	2404	3846	3906	

The baud rate can be set in UART mode within the following range.

### Table 21.4-2 Permissible Baud Rate Range in UART Mode

PSS[1:0]	BRS[7:0]
$00_{\rm B}$ to $11_{\rm B}$	$02_{\rm H}(2)$ to FF <sub>H</sub> (255)

### CHAPTER 21 UART/SIO DEDICATED BAUD RATE GENERATOR

# CHAPTER 22 LIN-UART

This chapter describes the function and operation of the LIN-UART

- 22.1 Overview of LIN-UART
- 22.2 Configuration of LIN-UART
- 22.3 LIN-UART Pins
- 22.4 Registers of LIN-UART
- 22.5 LIN-UART Interrupt
- 22.6 LIN-UART Baud Rate
- 22.7 Operations and Setting Procedure Example of LIN-UART
- 22.8 Notes on Using LIN-UART
- 22.9 Sample Programs of LIN-UART

### 22.1 Overview of LIN-UART

The LIN (Local Interconnect Network)-UART is a general-purpose serial data communication interface for synchronous or asynchronous (start-stop synchronization) communication with external devices. In addition to a bi-directional communication function (normal mode) and master/slave communication function (multiprocessor mode: supports both master and slave operation), the LIN-UART also supports the special functions used by the LIN bus.

### Functions of LIN-UART

The LIN-UART is a general-purpose serial data communication interface for exchanging serial data with other CPUs and peripheral devices. Table 22.1-1 lists the functions of the LIN-UART.

	Function
Data buffer	Full-duplex double-buffer
Serial input	The LIN-UART oversamples received data for five times to determine the received value by majority (only asynchronous mode).
Transfer mode	<ul> <li>Clock synchronization (Select start/stop synchronization, or start/stop bit)</li> <li>Clock asynchronous (Start/stop bits available)</li> </ul>
Baud rate	<ul> <li>Dedicated baud rate generator provided (made of a 15-bit reload counter)</li> <li>The external clock can be inputted. The reload counter can also be used to adjust the external clock.</li> </ul>
Data length	<ul><li> 7 bits (not in synchronous or LIN mode)</li><li> 8 bits</li></ul>
Signal type	NRZ (Non Return to Zero)
Start bit timing	Synchronization with the start bit falling edge in asynchronous mode.
Reception error detection	<ul> <li>Framing error</li> <li>Overrun error</li> <li>Parity error (Not supported in operation mode 1)</li> </ul>
Interrupt request	<ul> <li>Reception interrupts (reception completed, reception error detected, LIN synch break detected)</li> <li>Transmit interrupts (send data empty)</li> <li>Interrupt requests to TII0 (LIN synch field detected: LSYN)</li> </ul>
Master/slave mode communication function (Multiprocessor mode)	Capable of 1 (master) to n (slaves) communication (support both the master and slave system)
Synchronous mode	Send side/receive side of serial clock
Pin access	Serial I/O pin states can be read directly.
LIN bus option	<ul> <li>Master device operation</li> <li>Slave device operation</li> <li>LIN synch break detection</li> <li>LIN synch break generation</li> <li>Detection of LIN synch field start/stop edges connected to the 8/16-bit multifunction timer</li> </ul>
Synchronous serial clock	Continuous output to the SCK pin is possible for synchronous communication using the start/stop bits
Clock delay option	Special synchronous clock mode for delaying the clock (used for SPI)

Table 22.1-1 Functions of LIN-UART

The LIN-UART operates in four different modes. The operation mode is selected by the MD0 and MD1 bits in the LIN-UART serial mode register (SMR). Mode 0 and mode 2 are used for bi-directional serial communication; mode 1 for master/slave communication; and mode 3 for LIN master/slave communication.

Table 22.1-2 LIN-UART Operation Modes

Operation mode		Data	length	Synchronous	Stop bit length	Data hit format	
		No parity With parity		method		Data bit lonnat	
0	Normal mode	7 bits o	or 8 bits	Asynchronous	1 hit or 2 hite		
1	Multiprocessor mode	7 bits or 8 bits $+1^*$	-	Asynchronous	1 bit of 2 bits	LSB first MSB first	
2	Normal mode	8 bits		Synchronous	None, 1 bit, 2 bits		
3	LIN mode	8 bits	-	Asynchronous	1 bit	LSB first	

- : Unavailable

\* : "+1" is the address/data selection bit (A/D) used for communication control in multiprocessor mode.

The MD0 and MD1 bits in the LIN-UART serial mode register (SMR) are used to select the following LIN-UART operation modes.

Table 22.1-3 LIN-UART Operation Modes

MD1	MD0	Mode	Туре
0	0	0	Asynchronous (Normal mode)
0	1	1	Asynchronous (Multiprocessor mode)
1	0	2	Synchronous (Normal mode)
1	1	3	Asynchronous (LIN mode)

• Mode 1 supports both master and slave operation for the multiprocessor mode.

• Mode 3 is fixed to communication format 8-bit data, no parity, stop bit 1, LSB-first.

### 22.2 Configuration of LIN-UART

LIN-UART is made up of the following blocks.

- Reload counter
- Reception control circuit
- Reception shift register
- LIN-UART Reception data register (RDR)
- Transmit control circuit
- Transmit shift register
- LIN-UART Transmit data register (TDR)
- Error detection circuit
- Oversampling circuit
- Interrupt generation circuit
- LIN synch break/Synch Field detection circuit
- Bus idle detection circuit
- LIN-UART serial control register (SCR)
- LIN-UART serial mode register (SMR)
- LIN-UART Serial status register (SSR)
- LIN-UART Extended status control register (ESCR)
- LIN-UART Extended communication control register (ECCR)

### ■ LIN-UART Block Diagram



Figure 22.2-1 LIN-UART Block Diagram

#### Reload counter

This block is a 15-bit reload counter serving as a dedicated baud rate generator. The block consists of a 15-bit register for reload values; it generates the transmit/reception clock from the external or internal clock. The count value in the transmit reload counter is read from the baud rate generator (BGR 1 and BGR 0).

#### Reception control circuit

This block consists of a reception bit counter, a start bit detection circuit, and a reception parity counter. The reception bit counter counts the reception data bits and sets a flag in the LIN-UART reception data register when one data reception is completed according to the specified data length. If the reception interrupt is enabled at this time, a reception interrupt request is generated. The start bit detection circuit detects a start bit in a serial input signal. When a start bit is detected, the circuit sends a signal to the reload counter in synchronization with the start bit falling edge. The reception parity counter calculates the parity of the received data.

#### Reception shift register

The circuit inputs received data from the SIN pin while bit-shifting and transfers it to the RDR register upon completion of reception.

LIN-UART reception data register (RDR)

This register retains the received data. Serial input data is converted and stored in the LIN-UART reception data register.

### Transmit control circuit

This block consists of a transmit bit counter, a transmission start circuit, and a transmit parity counter. The transmit bit counter counts the transmit data bits and sets a flag in the transmit data register when one data transmission is completed according to the specified data length. If the transmit interrupt is enabled at this time, a transmit interrupt request is generated. The transmit start circuit starts transmission when data is written to the TDR. The transmit parity counter generates a parity bit for data to be transmitted if the data is parity-checked.

#### Transmit shift register

The data written to the LIN-UART transmit data register (TDR) is transferred to the transmit shift register, and output to the SOT pin while bit-shifting.

#### LIN-UART transmit data register (TDR)

This register sets the transmit data. The written data is converted to serial data and output.

#### Error detection circuit

This circuit detects an error upon completion of reception, if any. If an error occurs, the corresponding error flag is set.

### Oversampling circuit

In asynchronous mode, the LIN-UART oversamples received data for five times to determine the received value by majority. The LIN-UART stops during operation in synchronous mode.

#### Interrupt generation circuit

This circuit controls all interrupt factors. An interrupt is generated immediately if the corresponding interrupt enable bit has been set.

### LIN synch break/Synch Field detection circuit

This circuit detects a LIN synch break when the LIN master node transmits a message header. The LBD flag is set when the LIN synch break is detected. An internal signal is output to 8/16-bit compound timer in order to detect the first and fifth falling edges of the LIN synch Field and to measure the actual serial clock synchronization transmitted by the master node.

#### LIN synch break generation circuit

This circuit generates a LIN synch break with the specified length.

#### Bus idle detection circuit

This circuit detects that no transmission or reception is in progress, and generates the TBI and RBI flag bits.

#### LIN-UART serial control register (SCR)

Operating functions are as follows:

- Sets parity bit existence
- Parity bit selection
- Sets stop bit length
- Sets data length
- Selects the frame data format in mode 1
- · Clears error flag
- Enable/disable transmission
- Enables/disables reception

#### LIN-UART serial mode register (SMR)

Operating functions are as follows:

- Selects the LIN-UART operation mode
- Selects a clock input source
- Selects between one-to-one connection or reload counter connection for the external clock
- Resets a dedicated reload timer
- LIN-UART software reset (maintains register settings)
- Enables/disables output to the serial data pin
- Enables/disables output to the clock pin

LIN-UART serial status register (SSR)

Operating functions are as follows:

- Check transmission/reception or error status
- Selects the transfer direction (LSB-first or MSB-first)
- Enables/disables reception interrupts
- Enables/disables transmit interrupts

• Extended status control register (ESCR)

- Enables/disables LIN synch break interrupts
- LIN synch break detection
- Selects LIN synch break length
- Direct access to SIN pin and SOT pin
- Sets continuous clock output in LIN-UART synchronous clock mode
- Sampling clock edge selection

### LIN-UART extended communication control register (ECCR)

- Bus idle detection
- Synchronous clock setting
- LIN synch break generation

### ■ Input Clock

LIN-UART uses a machine clock or an input signal from the SCK pin as an input clock.

Input clock is used as clock source of transmission/reception of LIN-UART.

### This section describes LIN-UART pins.

### ■ LIN-UART Pins

The LIN-UART pins also serve as general-purpose ports. Table 22.3-1 lists the pin functions and settings for using the LIN-UART.

Pin name	Pin function	Required settings for using the pin
SIN	Serial data input	Set to the input port (DDR: corresponding bit = 0)
SOT	Serial data output	Set to output enable (SMR:SOE = 1)
SCK	Serial clock input/output	Set to the input port when used as clock input (DDR: corresponding bit = 0)
JCK	Serial clock input output	Set to output enable when used as clock output (SMR:SCKE = 1)

### Table 22.3-1 LIN-UART Pins

### Block Diagram of LIN-UART Pins



### Figure 22.3-1 Block Diagram of LIN-UART Pins (SCK, SOT, SIN)

### 22.4 Registers of LIN-UART

### This section lists the registers of LIN-UART.

### Register List of LIN-UART

		Figu	re 22.4	-1 Reg	ister Li	st of LIN	N-UART	m	
LIN-UART se	rial control reg	gister (S	CR)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0050 <sub>H</sub>	PEN	Р	SBL	CL	A/D	CRE	RXE	TXE	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R0,W	R/W	R/W	
LIN-UART se	rial mode regi	ster (SM	1R)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0051 <sub>H</sub>	MD1	MD0	OTO	EXT	REST	UPCL	SCKE	SOE	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R0,W	R0,W	R/W	R/W	
LIN-UART se	rial status reg	ister (SS	SR)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0052 <sub>H</sub>	PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE	00001000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/W	R/W	R/W	
LIN-UART re	ception data r	egister/t	ransmit (	data regi	ster (RD	R/TDR)			
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0053 <sub>H</sub>									00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
I IN-UART ex	tended status	control	register	(ESCR)					
Address	hit7	bit6	bit5	hit/	hit3	hit2	hit1	hit0	Initial value
0054					SOPE				
002 <del>4</del> H	R/W	R(RM1),W	R/W	R/W	R/W	R(RM1),W	R/W	R/W	00000100B
LIN-UART ex	tended comm	unicatio	n contro	l register	(ECCR)				
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0055 <sub>H</sub>	Reserved	LBR	MS	SCDE	SSM	Reserved	RBI	TBI	000000XX <sub>B</sub>
	R0/W	R0,W	R/W	R/W	R/W	R/W	R/WX	R/WX	
LIN-UART ba	ud rate gener	ator regi	ister 1 (E	3GR 1)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FBC <sub>H</sub>	-								00000000 <sub>B</sub>
	R0/W	R0,W	R/W	R/W	R/W	R/W	R/WX	R/WX	
LIN-UART ba	ud rate gener	ator regi	ister 0 (E	3GR 0)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
0FBD <sub>H</sub>									00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	_
R/W:	R/W: Readable/writable (Read value is the same as write value)								
R/WX:	Read only (F	Readable	e, writing	has no e	effect on	operatio	n)		
R(RM1), W:	Readable/wr	itable (R	lead valu	ue is diffe	erent fror	n write va	alue, "1"	is read by	read-modify-write
	(· ···· · / ····ou ·								

### 22.4.1 LIN-UART Serial Control Register (SCR)

The LIN-UART serial control register (SCR) is used to set parity, select the stop bit length and data length, select the frame data format in mode 1, clear the reception error flag, and enable/disable transmission/reception.

### ■ LIN-UART Serial Control Register (SCR)





	Bit name	Function
bit7	PEN: Parity enable bit	Specify whether or not to add (at transmission) and detect (at reception) a parity bit.         Note:       The parity bit is added only in operation mode 0, or in operation mode 2 with the settings that start/stop is set (ECCR:SSM = 1).         This bit is fixed to "0" in mode 3 (LIN).
bit6	P: Parity selection bit	Set either odd parity (1) or even parity (0) if the parity bit has been selected (SCR:PEN = 1).
bit5	SBL: Stop bit length selection bit	Set the bit length of the stop bit (frame end mark in transmit data) in operation mode 0, 1 (asynchronous) or in operation mode 2 (synchronous) with the settings that start/stop bit is set (ECCR:SSM = 1). This bit is fixed to "0" in mode 3 (LIN). Note: At reception, only the first bit of the stop bit is always detected.
bit4	CL: Data length selection bit	Specify the data length to be transmitted and received. This bit is fixed to "1" in mode 2 and mode 3.
bit3	A/D: Address/data format selection bit	Specify the data format for the frame to be transmitted and received in multiprocessor mode (mode 1). Write to this bit in master mode; read this bit in slave. The operation in master mode is as follows. "0": Set to data frame. "1": Set to address data frame. The value of last received data format is read. Note: See "22.8 Notes on Using LIN-UART" for using this bit.
bit2	CRE: Reception error flag clear bit	This bit is to clear FRE, ORE, and PE flags in serial status register (SSR). "0": No effect. "1": Clear the error flag. Reading this bit always returns "0". Note: Clear reception error flag after halting reception.
bit1	RXE: Reception operation enable bit	<ul> <li>Enable or disable the reception of LIN-UART.</li> <li>"0": Disable data frame reception.</li> <li>"1": Enable data frame reception.</li> <li>The LIN synch break detection in mode 3 is not affected.</li> <li>Note: When the reception is disabled (RXE = 0) during reception, the reception halts immediately. In that case, received data is not guaranteed.</li> </ul>
bit0	TXE: Transmit operation enable bit	<ul> <li>Enable or disable the transmission of LIN-UART.</li> <li>"0": Disable data frame transmission.</li> <li>"1": Enable data frame transmission.</li> <li>Note: When the transmission is disabled (TXE = 0) during transmission, the transmission halts immediately. In that case, received data is not guaranteed.</li> </ul>

Table 22.4-1 Functions of Each Bit in LIN-UART Serial Control Register (SCR)

### 22.4.2 LIN-UART Serial Mode Register (SMR)

The LIN-UART serial mode register (SMR) is used to select the operation mode, specify the baud rate clock, and enable/disable output to the serial data and clock pins.

### ■ LIN-UART Serial Mode Register (SMR)



Figure 22.4-3 LIN-UART Serial Mode Register (SMR)

Bit name Function								
		Set the operation mode. Note: If the mode is changed during communication, exchanging on LIN-UART halts and waits for starting the next communication.						
	MD1. MD0:	MD1 MD0 Mode Type						
bit7 bit6	Operation mode	0	0	0	Asynchronous (Normal mode)			
	selection bits	0	1	1	Asynchronous (Multiprocessor mode)			
		1	0	2	Synchronous (Normal mode)			
		1	1	3	Asynchronous (LIN mode)			
bit5	OTO: One-to-one external clock input enable bit	"1": Enable the external clock to be used directly as the LIN-UART serial clock. Used for reception side of serial clock (ECCR:MS = 1) in operation mode 2 (synchronous). When EXT = 0, the OTO bit is fixed to "0".						
bit4	EXT: External serial clock source selection bit	Select a clock input. "0": Select the clock of the internal baud rate generator (reload counter). "1": Select the external serial clock source.						
bit3	REST: Reload counter restart bit	Restart the reload counter. "0": No effect. "1": Restart the reload counter. Reading this bit always returns "0".						
bit2	UPCL: LIN-UART programmable clear bit (LIN-UART software reset)	<ul> <li>Reset the LIN-UART.</li> <li>"0": No effect.</li> <li>"1": Reset the LIN-UART immediately (LIN-UART software reset). However, the register settings are maintained. At that time, transmission and reception are halted. All of the transmit/reception interrupt factors (TDRE, RDRF, LBD, PE, ORE, FRE) are reset. Reset the LIN-UART after the interrupt and transmission are disabled. Also, the reception data register is cleared (RDR = 00<sub>H</sub>), and the reload counter is restarted.</li> </ul>						
bit1	SCKE: LIN-UART serial clock output enable bit	<ul> <li>Control the serial clock I/O port.</li> <li>"0": The SCK pin works as a general-purpose I/O port or a serial clock input pin.</li> <li>"1": This pin works as the serial clock output pin and outputs the clock in operation mode 2 (synchronous).</li> <li>Note: When the SCK pin is used as a serial clock input (SCKE = 0), set the corresponding DDR bits in the general-purpose I/O port as an input port. Also, select the external clock (EXT = 1) by using the clock selection bit.</li> <li>When the SCK pin is set as a serial clock output (SCKE = 1), this pin works as a serial clock output pin regardless of the state of the general-purpose I/O port</li> </ul>						
bit0	SOE: LIN-UART serial data output enable bit	<ul> <li>Enable or disable output of serial data.</li> <li>"0": The SOT pin works as a general-purpose I/O port.</li> <li>"1": The SOT pin works as a serial data output pin (SOT).</li> <li>When set as a serial data output (SOE = 1), the SOT pin works as a SOT pin regardless of a general-purpose I/O port.</li> </ul>						

### Table 22.4-2 Functions of Each Bit in LIN-UART Serial Mode Register (SMR)

### 22.4.3 LIN-UART Serial Status Register (SSR)

The LIN-UART serial status register (SSR) is used to check the status of transmission/ reception or error, and to enable/disable interrupts.

### ■ LIN-UART Serial Status Register (SSR)



Figure 22.4-4 LIN-UART Serial Status Register (SSR)

	Bit name	Function
bit7	PE: Parity error flag bit	<ul> <li>Detect a parity error in received data.</li> <li>This bit is set to "1" when a parity error occurs during reception with PE = 1, and cleared by writing "1" to the CRE bit in the LIN-UART serial control register (SCR).</li> <li>Output a reception interrupt request when both PE bit and RIE bit are "1".</li> <li>When this flag is set, the data in the reception data register (RDR) is invalid.</li> </ul>
bit6	ORE: Overrun error flag bit	<ul> <li>Detect an overrun error in received data.</li> <li>This bit is set to "1" when an overrun occurs during reception, and cleared by writing "1" to the CRE bit in the LIN-UART serial control register (SCR).</li> <li>Output a reception interrupt request when both ORE bit and RIE bit are "1".</li> <li>When this flag is set, the data in the reception data register (RDR) is invalid.</li> </ul>
bit5	FRE: Framing error flag bit	<ul> <li>Detect a framing error in received data.</li> <li>This bit is set to "1" when a framing error occurs during reception, and cleared by writing "1" to the CRE bit in the LIN-UART serial control register (SCR).</li> <li>Output a reception interrupt request when both FRE bit and RIE bit are "1".</li> <li>When this flag is set, the data in the LIN-UART reception data register (RDR) is invalid.</li> </ul>
bit4	RDRF: Reception data full flag bit	<ul> <li>This flag shows the status of the LIN-UART reception data register (RDR).</li> <li>This bit is set to "1" when received data is loaded into RDR, and cleared to "0" by reading the reception data register (RDR).</li> <li>Output a reception interrupt request when both RDRF bit and RIE bit are "1".</li> </ul>
bit3	TDRE: Transmit data empty flag bit	<ul> <li>This flag shows the status of the LIN-UART transmit data register (TDR).</li> <li>This bit is set to "0" by writing the transmit data to TDR, and indicates that the TDR has valid data. This bit is set to "1" when data is loaded into the transmit shift register and transferred, and indicates that the TDR does not have effective data.</li> <li>Output a transmit interrupt request when both TDRE bit and TIE bit are "1".</li> <li>When the TDRE bit is "1", setting the LBR bit in the LIN-UART extended communication control register (ECCR) to "1" changes the TDRE bit to "0". Then, the TDRE bit goes back to "1" after LIN synch break is generated.</li> <li>Note: The initial state is TDRE =1.</li> </ul>
bit2	BDS: Transfer direction selection bit	Specify whether the transfer serial data is transfer from the least significant bit (LSB-first, BDS = 0) or from the most significant bit (MSB-first, BDS = 1).         Note:       Since data values are exchanged between the upper and lower when the data is read/written to the serial data register, changing BDS bit after writing data to the RDR register invalidates the written data. The BDS bit is fixed to "0" in mode 3 (LIN).
bit1	RIE: Reception interrupt request enable bit	Enable or disable the reception interrupt request output to the interrupt controller. Output a reception interrupt request when both the RIE bit and the reception data flag bit (RDRF) are "1", or when one or more error flag bits (PE, ORE, FRE) is "1".
bit0	TIE: Transmit interrupt request enable bit	Enable or disable the transmit interrupt request output to the interrupt controller. Output a transmit interrupt request when both TIE bit and TDRE bit are "1".

Table 22.4-3 Functions of Each Bit in Serial Status Register (SSR)

### 22.4.4 LIN-UART Reception Data Register/LIN-UART Transmit Data Register (RDR/TDR)

The LIN-UART reception and LIN-UART transmit data registers are located at the same address. If read, they work as the reception data register; if written, they work as the transmit data register.

### ■ LIN-UART Reception Data Register (RDR)

Figure 22.4-5 shows the bit configuration of LIN-UART reception/LIN-UART transmit data register.





The LIN-UART reception data register (RDR) is the data buffer register for the serial data reception.

Serial input data signal transmitted to the serial input pin (SIN pin) is converted via a shift register and stored in the LIN-UART reception data register (RDR).

If the data length is 7 bits, the upper 1 bit (RDR:D7) is "0".

The reception data full flag bit (SSR:RDRF) is set to "1" when received data is stored into the LIN-UART reception data register (RDR). If the reception interrupt is enabled (SSR:RIE = 1), a reception interrupt request is generated.

The LIN-UART reception data register (RDR) should be read when the reception data full flag bit (SSR:RDRF) is "1". The reception data full flag bit (SSR:RDRF) is automatically cleared to "0" by reading the LIN-UART reception data register (RDR). Also, the reception interrupt is cleared when the reception interrupt is enabled and no error occurs.

When the reception error occurs (any of SSR:PE, ORE, or FRE is "1"), the data in the LIN-UART reception data register (RDR) is invalid.

### ■ LIN-UART Transmit Data Register (TDR)

The LIN-UART transmit data register (TDR) is the data buffer register for the serial data transmission.

If the data to be transmitted is written to the LIN-UART transmit data register (TDR) when transmission is enabled (SCR:TXE = 1), the transmit data is transferred to the transmission shift register, converted to serial data, and output from the serial data output pin (SOT pin).

If the data length is 7 bits, the data in the upper 1 bit (TDR:D7) is invalid.

The transmit data empty flag (SSR:TDRE) is cleared to "0" when a transmit data is written to the LIN-UART transmit data register (TDR).

The transmit data empty flag (SSR:TDRE) is set to "1" after the data is transferred to the transmission shift register and the transmission starts.

If the transmit data empty flag (SSR:TDRE) is "1", the next transmit data can be written. If the transmit interrupt is enabled, a transmit interrupt is generated. The next transmit data should be written by generating the transmit interrupt, or when the transmit data empty flag (SSR:TDRE) is "1".

Note:

The LIN-UART transmit data register is a write-only register; the reception data register is a readonly register. Since both registers are located at the same address, the write value and read value are different. Thus, the instructions to operate the read-modify-write (RMW) instruction, such as the INC/DEC instruction, cannot be used.

### 22.4.5 LIN-UART Extended Status Control Register (ESCR)

The LIN-UART extended status control register (ESCR) has the settings for enabling/ disabling LIN synch break interrupt, LIN synch break length selection, LIN synch break detection, direct access to the SIN and SOT pins, continuos clock output in LIN-UART synchronous clock mode and sampling clock edge.

### ■ Bit Configuration of LIN-UART Extended Status Control Register (ESCR)

Figure 22.4-6 shows the bit configuration of the LIN-UART extended status control register (ESCR). Table 22.4-4 lists the function of each bit.



### Figure 22.4-6 Bit Configuration of LIN-UART Extended Status Control Register (ESCR)

	Bit name	Function
bit7	LBIE: LIN synch break detection interrupt enable bit	This bit enables or disables LIN synch break detection interrupts. An interrupt is generated when the LIN synch break detection flag (LBD) is "1" and the interrupt is enabled (LBIE = 1). This bit is fixed to "0" in mode 1 and mode 2.
bit6	LBD: LIN synch break detection flag bit	Detect LIN synch break.         This bit is set to "1" when the LIN synch break is detected in operation mode 3 (the serial input is "0" when bit width is 11 bits or more). Also, writing "0" clears the LBD bit and the interrupt. Although the bit is always read as "1" when the read-modify-write (RMW) instruction is executed, this does not indicate that a LIN synch break detected.         Note:       To detect a LIN synch break, enable the LIN synch break detection interrupt (LBIE = 1), and then disable the reception (SCR:RXE = 0).
bit5 bit4	LBL1/LBL0: LIN synch break length selection bits	These bits specify the bit length for the LIN synch break generation time. The LIN synch break length for reception is always 11 bits.
bit3	SOPE: Serial output pin direct access enable bit <sup>*</sup>	Enable or disable direct writing to the SOT pin. Setting this bit to "1" when serial data output is enabled (SMR:SOE = 1) enables direct writing to the SOT pin.*
bit2	SIOP: Serial I/O pin direct access bit <sup>*</sup>	Control direct access to the serial I/O pin. Normal read instruction always returns the value of the SIN pin. When direct access to the serial output pin data is enabled (SOPE = 1), the SOT pin reflects the value written to this bit. Note: The bit operation instruction returns the bit value of the SOT pin in the read cycle. <sup>*</sup>
bit1	CCO: Continuous clock output enable bit	Enable or disable continuous serial clock output from the SCK pin. Setting this bit to "1" with sending side of serial clock in operation mode 2 (synchronous) enables the continuous serial clock output from the SCK pin if the pin is set as a clock output. Note: When the CCO bit is "1", the SSM bit in the ECCR should be "1".
bit0	SCES: Sampling clock edge selection bit	Select a sampling edge. Setting the SCES to "1" in reception side of serial clock in operation mode 2 (synchronous) switches the sampling edge from the rising edge to the falling edge. When the SCK pin is set as the clock output with sending side of serial clock (ECCR:MS = 0) in operation mode 2, the internal serial clock and the output clock signal are inverted. This bit should be "0" in operation modes 0, 1, and 3.

### Table 22.4-4 Functions of Each Bit in LIN-UART Extended Status Control Register (ESCR)

### \*: Interaction between SOPE and SIOP

SOPE	SIOP	Write to SIOP	Read from SIOP					
0	R/W	No effect (however, the write value is retained)	Return the SIN value					
1	R/W	Write "0" or "1" to SOT	Return the SIN value					
1	RMW	Read the SOT value, write "0" or "1"						

# 22.4.6 LIN-UART Extended Communication Control Register (ECCR)

The LIN-UART extended communication control register (ECCR) is used for the bus idle detection, the synchronous clock setting, and the LIN synch break generation.

### Bit Configuration of LIN-UART Extended Communication Control Register (ECCR)

Figure 22.4-7 shows the bit configuration of the LIN-UART extended communication control register (ECCR). Table 22.4-5 lists the function of each bit.





Bit name		Function					
bit7	Reserved bit	The read value is indeterminate. "0" is always set.					
bit6	LBR: LIN synch break generation bit	Setting this bit to "1" in mode 3 generates a LIN synch break which has the length specified by LBL 0/1 in the ESCR. This bit should be "0" in mode 0, 1 and 2.					
bit5	MS: Sending side/receiving side of serial clock selection bit	<ul> <li>Select sending side/receiving side of serial clock in mode 2.</li> <li>When sending side "0" is selected, generate a synchronous clock.</li> <li>When receiving side "1" is selected, receive an external serial clock. This bit is fixed to "0" in modes 0, 1, and 3.</li> <li>Modify this bit only when the SCR:TXE bit is "0".</li> <li>Note: When receiving side is selected, the clock source must be set as an external clock and the external clock input must be enabled (SMR:SCKE = 0, EXT = 1, OTO = 1).</li> </ul>					
bit4	SCDE: Serial clock delay enable bit	Setting the SCDE bit to "1" at sending side/receiving side of serial clock in mode 2 outputs a delayed serial clock as shown in Figure 22.7-5. This bit is effective in SPI. This bit is fixed to "0" in modes 0, 1, and 3.					
bit3	SSM: Start/stop bit mode enable bit	Add the start/stop bit to the synchronous data format when this bit is set to "1" in mode 2. This bit is fixed to "0" in modes 0, 1, and 3.					
bit2	Reserved bit	The read value is indeterminate. "0" is always set.					
bit1	RBI: Reception bus idle detection flag bit	When the SIN pin is "H" level and reception is not performed, this bit is "1". Do not use this bit when $SSM = 0$ in operation mode 2.					
bit0	TBI: Transmit bus idle detection flag bit	This bit is "1" when there is no transmission on the SOT pin. Do not use this bit when $SSM = 0$ in operation mode 2.					

### Table 22.4-5 Functions of Each Bit in LIN-UART Extended Communication Control Register (ECCR)

### 22.4.7 LIN-UART Baud Rate Generator Register 0, 1 (BGR 0/1)

The LIN-UART baud rate generator register 0, 1 (BGR 0/1) sets the division ratio of the serial clock. Also, the count value in the transmit reload counter is read from this generator.

### ■ LIN-UART Bit Configuration of Baud Rate Generator Register (BGR 0/1)

Figure 22.4-8 shows the bit configuration of LIN-UART baud rate generator register (BGR 0/1).



#### Figure 22.4-8 Bit Configuration of LIN-UART Baud Rate Generator Register (BGR 0/1)

The LIN-UART baud rate generator register sets the division ratio of the serial clock.

BGR 1 is associated with the upper bits; BGR 0 is associated with the lower bits. The reload value of the counter can be written and the transmit reload counter value can be read from them. Byte/word access is also possible.

Writing a reload value to the LIN-UART baud rate generator registers causes the reload counter to start counting.

### Note:

Write to this register when LIN-UART stops.

### 22.5 LIN-UART Interrupt

The LIN-UART has reception interrupts and transmit interrupts, which are generated by following factor and have the assigned interrupt number and interrupt vector. Also, it has the LIN synch field edge detection interrupt function using the 8/16-bit compound timer interrupt.

- Reception interrupts
   When the received data is set in the LIN-UART reception data register (RDR), or when a reception error occurs. Also, when a LIN synch break is detected.
- Transmit interrupts
   When the transmit data is transferred from the LIN-UART transmit data register (TDR) to the transmission shift register, and the transmission starts.

### Reception Interrupt

Table 22.5-1 shows the control bits and interrupt factors of reception interrupts.

Table 22.5-1 Interrupt Control Bits and Interrupt Factors of Reception Interrupts

Interrupt	Flag register	Operation mode		ode		Interrupt factor		
bit		0	1	2	3	Interrupt lactor	enable bit	interrupt request hag clear
RDRF	SSR	0	0	О	0	Write received data to RDR		Read received data
ORE	SSR	0	0	О	0	Overrun error	SSR:RIE	Write "1" to reception error flag clear bit (SCR:CRE)
FRE	SSR	0	0	$\Delta$	0	Framing error		
PE	SSR	0	×	$\Delta$	×	Parity error		
LBD	ESCR	×	×	×	0	LIN synch break detection	ESCR:LBIE	Write "0" to ESCR:LBD

O: Used bit

× : Unused bit

 $\Delta$ : Only ECCR/SSM = 1 available

### Reception interrupts

Each flag bit in the LIN-UART serial status register (SSR) is set to "1" when any of following operation occurs in reception mode:

### Data reception completed

When the reception data is transferred from the LIN-UART serial input shift register to the LIN-UART reception data register (RDR) (RDRF = 1)

### **Overrun error**

When the following serial data is received when RDRF = 1 and the RDR is not read by the CPU (ORE = 1)

### **Framing error**

When the stop bit reception error occurs (FRE = 1)

### Parity error

When the parity detection error occurs (PE = 1)

A reception interrupt request is generated if the reception interrupt is enabled (SSR:RIE = 1) when any of the above flag bits is "1".

RDRF flag is automatically cleared to "0" by reading the LIN-UART reception data register (RDR). All of error flags are cleared to "0" by writing "1" to the reception error flag clear bit (CRE) in the LIN-UART serial control register (SCR).

#### Note:

CRE flag is write-only, and retains "1" for one clock cycle when "1" is written.

LIN synch break interrupts

Works for LIN slave operation in operation mode 3.

The LIN synch break detection flag bit (LBD) in the LIN-UART extended status control register (ESCR) is set to "1" when the internal data bus (serial input) is "0" for 11 bits or longer. The LIN synch break interrupt and the LBD flag are cleared by writing "0" to the LBD flag. The LBD flag must be cleared before the 8/16-bit compound timer interrupt is generated in the LIN synch field.

To detect a LIN synch break, the reception must be disabled (SCR:RXE = 0).

### Transmit Interrupts

Table 22.5-2 shows the control bits and interrupt factors of transmit interrupts.

#### Table 22.5-2 Interrupt Control Bits and Interrupt Factors of Transmit Interrupts

Interrupt	Flag register	Operation mode			de		Interrupt factor	
bit		0	1	2	3	interrupt lactor	enable bit	interrupt request hag clear
TDRE	SSR	О	О	О	0	Transmit register is empty	SSR:TIE	Write transmit data

O: Used bit

Transmit interrupts

The transmit data register empty flag bit (TDRE) in the LIN-UART serial status register (SSR) is set to "1" when the transmit data is transferred from the LIN-UART transmit data register (TDR) to the transmission shift register, and the transmission starts. If the transmit interrupt is enabled (SSR:TIE = 1) in this case, a transmit interrupt request is generated.

#### Note:

Since the initial value of TDRE is "1", an interrupt is generated immediately after the TIE bit is set to "1" after hardware/software reset. Also, the TDRE is cleared only by writing data to the LIN-UART transmit data register (TDR).

### ■ LIN Synch Field Edge Detection Interrupt (8/16-bit Compound Timer Interrupt)

Table 22.5-3 shows the control bits and interrupt factors of the LIN synch field edge detection interrupt.

Table 22.5-3	Interrupt Control	Bits and Interrup	ot Factors of LIN S	vnch Field Edae	e Detection Interrupt
				,	

Interrupt	Flag	Operation mode			ode	Interrupt factor	Interrupt factor	Interrupt request flag
request flag bit	register	0	1	2	3	menupriación	enable bit	clear
IR	T00CR1	×	×	×	0	First falling edge of the LIN synch field	TOOCP1.IE	Write "0" to TOOCP1.IP
IR	T00CR1	×	×	×	0	Fifth falling edge of the LIN synch field	TUUCKI.IE	WINE 0 10 IUUCKI.IK

O: Used bit

 $\times$  : Unused bit

### • LIN Synch field edge detection interrupt (8/16-bit compound timer interrupt)

Works for LIN slave operation in operation mode 3.

After a LIN synch break is detected, the internal signal (LSYN) is set to "1" at the first falling edge of the LIN synch field, and set to "0" after the fifth falling edge. When the 8/16-bit compound timer is configured to be input the internal signal and to detect both edges, a 8/16-bit compound timer interrupt is generated if enabled.

The difference in the count values detected by the 8/16-bit compound timer (see Figure 22.5-1) corresponds to the 8 bits in the master serial clock. The new baud rate can be calculated from this value.

When a new baud rate is set, the rate become effective from the falling edge detection of the specified next start bit.





### ■ Register and Vector Table Related to LIN-UART Interrupt

Interrupt factor	Interrupt	Interrupt level	setting register	Address of vector table		
	request No.	Register	Setting bit	Upper	Lower	
Reception	IRQ7	ILR1	L07	FFFC <sub>H</sub>	FFFD <sub>H</sub>	
Transmission	IRQ8	ILR2	L08	FFEA <sub>H</sub>	FFEB <sub>H</sub>	

### Table 22.5-4 Register and Vector Table Related to LIN-UART Interrupt

### 22.5.1 Timing of Reception Interrupt Generation and Flag Set

## Reception interrupts are a reception completion (SSR:RDRF) and an occurrence of a reception error (SSR:PE, ORE, FRE).

### Timing of Reception Interrupt Generation and Flag Set

Received data is stored in the LIN-UART reception data register (RDR) when the first stop bit is detected in mode 0, 1, 2 (SSM =1), 3, or when the last data bit is detected in mode 2 (SSM = 0). Each error flag is set when a reception is completed (SSR:RDRF = 1), or when a reception error occurs (SSR:PE, ORE, FRE = 1). If the reception interrupt is enabled (SSR:RIE = 1) at this time, a reception interrupt is generated.

Note:

When a reception error occurs in each mode, the data in the LIN-UART reception data register (RDR) is invalid.

Figure 22.5-2 shows the timing of reception and flag set.



Figure 22.5-2 Timing of Reception and Flag Set

Note:

Figure 22.5-2 does not show all receptions in mode 0. It only shows examples for 7-bit data, parity (even parity or odd parity), 1 stop bit and 8-bit data, no parity, 1 stop bit.



### 22.5.2 Timing of transmit interrupt generation and flag set

Transmit interrupts are generated when the transmit data is transferred from the LIN-UART transmit data register (TDR) to the transmission shift register and then the transmission starts.

### Timing of Transmit Interrupt Generation and Flag Set

When the data written to the LIN-UART transmit data register (TDR) is transferred to the transmission shift register and then the transmission starts, the next data becomes to be writable (SSR:TDRE = 1). If the transmit interrupt is enabled (SSR:TIE = 1) at this time, a transmit interrupt is generated.

TDRE bit is a read-only bit and cleared to "0" only by writing data to the LIN-UART transmit data register (TDR).

Figure 22.5-4 shows the timing of the transmission and flag set in each LIN-UART mode.



#### Figure 22.5-4 Timing of Transmission and Flag Set

Note:

Figure 22.5-4 does not show all transmissions in mode 0. It only shows 8-bit data, parity ("even parity" or "odd parity"), 1 stop bit.

No parity bit is transmitted in mode 3, or in mode 2 with SSM = 0.

### ■ Transmit Interrupt Request Generation Timing

When TDRE flag is set to "1" if the transmit interrupt is enabled (SSR:TIE = 1), a transmit interrupt request is generated.

### Note:

Since the TDRE bit is initially set to "1", a transmit interrupt is generated immediately after the transmit interrupt is enabled (SSR:TIE = 1). Be careful with the timing for enabling the transmit interrupt since the TDRE bit can be cleared only by writing new data to the LIN-UART transmit data register (TDR).

Refer to "APPENDIX B Table of Interrupt Causes" for interrupt request number/vector table of each peripheral function.

### 22.6 LIN-UART Baud Rate

One of the following can be selected for the LIN-UART input clock (send/receive clock source):

- Input a machine clock into a baud rate generator (reload counter)
- Input an external clock into a baud rate generator (reload counter)
- Use the external clock (SCK pin input clock) directly.

### ■ LIN-UART Baud Rate Selection

You can select one of the following three different baud rates. Figure 22.6-1 shows the baud rate selection circuit.

• Baud rate derived from the internal clock divided by the dedicated baud rate generator (reload counter)

Two internal reload counters are provided and assigned the transmit and reception serial clock respectively. The baud rate is selected by setting a 15-bit reload value in the LIN-UART baud rate generator register 1, 0 (BGR1, BGR0).

The reload counter divides the internal clock by the specified value.

It is used in asynchronous mode and in synchronous mode (sending side of serial clock).

To set the clock source, select the use of the internal clock and baud rate generator (SMR:EXT = 0, OTO = 0).

• Baud rate derived from the external clock divided by the dedicated baud rate generator (reload counter)

The external clock is used as the clock source for the reload counter.

The baud rate is selected by setting a 15-bit reload value in the LIN-UART baud rate generator register 1, 0 (BGR0, BGR1).

The reload counter divides the external clock by the specified value.

It is used in asynchronous mode.

To set the clock source, select the use of the external clock and baud rate generator (SMR:EXT = 1, OTO = 0).

Baud rate by the external clock (one-to-one mode)

The clock input from the clock input pin (SCK) of the LIN-UART is used as the baud rate (slave 2 operation (ECCR:MS =1) in synchronous mode).

It is used in synchronous mode (receiving side of serial clock).

To set the clock source, select the external clock and its direct use (SMR:EXT = 1, OTO = 1).


Figure 22.6-1 LIN-UART Baud Rate Selection Circuit

### 22.6.1 Baud Rate Setting

# This section shows baud rate settings and the calculation result of serial clock frequencies.

#### Baud Rate Calculation

The two 15-bit reload counters are set by the LIN-UART baud rate generator register 1, 0 (BGR 1, BGR 0). The expressions for the baud rate are as follows.

Reload value:

v = (MCLK/b) - 1

v: Reload value, b: Baud rate, MCLK: Machine clock, or external clock frequency

#### **Calculation example**

Assuming that the machine clock is 10MHz, the internal clock is used, and the baud rate is set to 19200 bps:

Reload value:

$$v = \left(\frac{10 \times 10^6}{19200}\right) -1 = 520.83 \dots 520$$

Thus, the actual baud rate can be calculated as follows.

$$b = \frac{MCLK}{(v+1)} = \frac{10 \times 10^6}{521} = 19193.8579$$

Note:

The reload counter halts if the reload value is set to "0". Therefore, the least reload value should be "1".

For transmission/reception in asynchronous mode, the reload value must be at least "4" in order to determine the reception value by oversampling on five times.

### ■ Reload Value and Baud Rate of Each Clock Speed

Table 22.6-1 shows the reload value and baud rate of each clock speed.

Table 22.6-1 Reload Value and Baud Rate

Doud	8MHz	z (MCLK)	10MH	z (MCLK)	16MH	16MHz (MCLK)		16.25MHz(MCLK)	
rate	Reload value	Frequency deviation							
2M	_	-	4	0	7	0	_	-	
1M	7	0	9	0	15	0	_	_	
500000	15	0	19	0	31	0	-	_	
400800					-	_	-	-	
250000	31	0	39	0	63	0	64	0	
230400					68	- 0.64	-	-	
153600	51	- 0.16	64	- 0.16	103	- 0.16	105	0.19	
125000	63	0	79	0	127	0	129	0	
115200	68	- 0.64	86	0.22	138	0.08	140	- 0.04	
76800	103	0.16	129	0.16	207	- 0.16	211	0.19	
57600	138	0.08	173	0.22	277	0.08	281	- 0.04	
38400	207	0.16	259	0.16	416	0.08	422	- 0,04	
28800	277	0.08	346	- 0.06	555	0.08	563	- 0.04	
19200	416	0.08	520	0.03	832	- 0.04	845	- 0.04	
10417	767	< 0.01	959	< 0.01	1535	< 0.01	1559	< 0.01	
9600	832	- 0.04	1041	0.03	1666	0.02	1692	0.02	
7200	1110	< 0.01	1388	< 0.01	2221	< 0.01	2256	< 0.01	
4800	1666	0.02	2082	- 0.02	3332	< 0.01	3384	< 0.01	
2400	3332	< 0.01	4166	< 0.01	6666	< 0.01	6770	< 0.01	
1200	6666	< 0.01	8334	< 0.01	13332	< 0.01	13541	< 0.01	
600	13332	< 0.01	16666	< 0.01	26666	< 0.01	27082	< 0.01	
300	26666	< 0.01	_	-	53332	< 0.01	54166	< 0.01	

The unit of frequency deviation (dev.) is %. MCLK indicates the machine clock.

#### External Clock

The external clock is selected by writing "1" to the EXT bit in the LIN-UART serial mode register (SMR). In the baud rate generator, the external clock can be used in the same way as the internal clock.

When slave operation is used in synchronous mode 2, select the one-to-one external clock input mode (SMR:OTO = 1). In this mode, the external clock input to SCK is input directly to the LIN-UART serial clock.

#### Note:

The external clock signal is synchronized with the internal clock (MCLK: machine clock) in the LIN-UART. Therefore, the signal is unstable because the external clock cannot be divided if its cycle is faster than half cycle of the internal clock.

For the value of the SCK clock, refer to the data sheet.

#### ■ Operation of Dedicated Baud Rate Generator (Reload Counter)

Figure 22.6-2 shows the operation of two reload counters when the reload value is "832 as an example".

#### Figure 22.6-2 Operation of Dedicated Baud Rate Generator (Reload Counter)



#### Note:

The falling edge of the serial clock signal is generated after the reload value divided by 2 ((V+1)/2) is counted.

## 22.6.2 Reload Counter

# This block is a 15-bit reload counter serving as a dedicated baud rate generator. It generates the transmit/reception clock from the external or internal clock. The count value in the transmit reload counter is read from the LIN-UART baud rate generator registers (BGR 1 and BGR 0).

#### Function of Reload Counter

There are two kinds of reload counters; transmit and reception. They work as the dedicated baud rate generator. The block consists of a 15-bit register for reload values; it generates the transmit/reception clock from the external or internal clock. The count value in the transmit reload counter is read from the LIN-UART baud rate generator registers (BGR 1 and BGR 0).

#### Start counting

Writing a reload value to the LIN-UART baud rate generator registers (BGR 1, BGR 0) causes the reload counter to start counting.

#### Restart

The reload counter restarts in the following conditions.

For both transmit/reception reload counter

- LIN-UART programmable reset (SMR:UPCL bit)
- Programmable restart (SMR:REST bit)

For reception reload counter

Start bit falling edge detection in asynchronous mode

#### Simple timer function

Two reload counters restart at the next clock cycle when the REST bit in the LIN-UART serial mode register (SMR) is set to "1".

This function enables the transmit reload counter to be used as a simple timer.

Figure 22.6-3 shows an example of using this function (when reload value is 100).



The number of machine cycles "cyc" after restart in this example is obtained by the following expression. cyc = v - c + 1 = 100 - 90 + 1 = 11

v: Reload value, c: Reload counter value

#### Note:

The reload counters also restart when the LIN-UART is reset by writing "1" to the SMR:UPCL bit.

Automatic restart (reception reload counter only)

The reception reload counter is restarted when the start bit falling edge is detected in asynchronous mode. This is the function to synchronize the reception shift register with the reception data.

#### Clear counter

When a reset occurs, the reload values in the LIN-UART baud rate generator registers (BGR 1, BGR 0) and the reload counter are cleared to " $00_{\text{H}}$ ", and the reload counter halts.

Although the counter value is temporarily cleared to  $"00_{\text{H}}"$  by the LIN-UART reset (writing "1" to SMR:UPCL), the reload counter restarts since the reload value is retained.

The counter value is not cleared to " $00_{\text{H}}$ " by the reset setting (writing "1" to SMR:REST), and the reload counter restarts.

# 22.7 Operations and Setting Procedure Example of LIN-UART

LIN-UART operates in mode 0, 2 for bi-directional serial communication, in mode 1 for master/slave communication, and in mode 3 for LIN master/slave communication.

#### Operation of LIN-UART

#### • Operation mode

The LIN-UART has four operation modes (0 to 3), allowing the connections and the data transfer methods between CPUs to be selected as listed in Table 22.7-1.

Table 22.7-1 LIN-UART Operation Modes

Operation mode		Data length		Synchronous method	Stop bit length	Data hit format
		No parity	With parity	Synchronous method	Stop bit length	Data bit ionnat
0	Normal mode	7 bits or 8 bits		Asynchronous		
1	Multiprocessor mode	7 bits or 8 bits $+1^*$	-	Asynchronous	1 bit or 2 bits	LSB first MSB first
2	Normal mode	8 bits		Synchronous	None, 1 bit, 2 bits	
3	LIN mode	8 bits	-	Asynchronous	1 bit	LSB first

- : Unavailable

\*: "+1" is the address/data selection bit (A/D) used for communication control in multiprocessor mode.

The MD0 and MD1 bits in the LIN-UART serial mode register (SMR) are used to select the following LIN-UART operation modes.

#### Table 22.7-2 LIN-UART Operation Modes

MD1	MD0	Mode	Туре
0	0	0	Asynchronous (Normal mode)
0	1	1	Asynchronous (Multiprocessor mode)
1	0	2	Synchronous (Normal mode)
1	1	3	Asynchronous (LIN mode)

Notes:

- Both master and slave operation are supported in a system with master/slave connection in mode 1.
- In mode 3, the communication format is fixed to 8-bit data, no parity, stop bit1, LSB-first.
- If the mode is changed, all transmissions and receptions are canceled, and the LIN-UART waits for the next operation.

#### Inter-CPU Connection Method

You can select either external clock one-to-one connection (normal mode) or master/slave connection (multiprocessor mode). In either methods, data length, parity setting, synchronization type must be the same between all CPUs and thus the operation mode must be selected as follows.

- One-to-one connection: Two CPUs must use the same method in either operation mode 0 or 2. Select the operation mode 0 for asynchronous method or the operation mode 2 for synchronous method. Also, for the operation mode 2, set one CPU as sending side of serial clock and the other as the receiving side of serial clock.
- Master/slave connection: Select operation mode 1. Use the system as a master/slave system.

#### Synchronous Method

In asynchronous method, the reception clock is synchronized with the reception start bit falling edge. In synchronous method, the reception clock can be synchronized by the sending side of serial clock signal or the clock signal at operating as sending side of serial clock.

#### ■ Signaling

NRZ (Non Return to Zero).

#### Enable Transmission/Reception

The LIN-UART uses the SCR:TXE bit and the SCR:RXE bit to control transmission and reception, respectively. To disable transmission or reception, set as follows.

- If the reception is in progress, wait until the reception completed, read the LIN-UART reception data register (RDR), and then disable the reception.
- If the transmission is in progress, wait until the transmission completed, and then disable the transmission.

#### Setting Procedure

LIN-UART is set in the following procedure:

- Initial setting
  - 1) Set the port input (DDR1).
  - 2) Set the interrupt level (ILR1, ILR2).
  - 3) Set the data format, enable transmission/reception (SCR).
  - 4) The operation mode, baud rate selection, pin output enabled (SMR)
  - 5) The baud rate generator (BGR1,BGR0)

# 22.7.1 Operation of Asynchronous Mode (Operation Mode 0, 1)

# When LIN-UART is used in operation mode 0 (normal mode) or operation mode 1 (multiprocessor mode), the transfer method is asynchronous.

#### Asynchronous Mode Operation

#### Transmit/reception data format

Transmit/reception data always begins with a start bit ("L" level) followed by a specified data bits length and ends up with at least one stop bit ("H" level).

The bit transfer direction (LSB-first or MSB-first) is determined by the BDS bit in the LIN-UART serial status register (SSR). When a parity is used, the parity bit is always placed between the last data bit and the first stop bit.

In operation mode 0, select 7-bit or 8-bit for the data length. You can select whether or not to use a parity. Also, the stop bit length (1 or 2) can be selected.

In operation mode 1, a data length is 7-bit or 8-bit, the parity is not added, and the address/data bit is added. The stop bit length (1 or 2) can be selected.

The bit length of transmit/reception frame is calculated as follows:

Length = 1 + d + p + s

(d = Number of data bits [7 or 8], p = parity [0 or 1],

s = Number of stop bits [1 or 2])

Figure 22.7-1 shows the data format in asynchronous mode.



Figure 22.7-1 Transmit/Reception Data Format (Operation Mode 0, 1)

#### Note:

When the BDS bit in the LIN-UART serial status register (SSR) is set to "1" (MSB-first), the bits are processed in the order of D7, D6, ... D1, D0 (P).

#### Transmission

If the transmit data register empty flag bit (TDRE) in the LIN-UART serial status register (SSR) is "1", transmit data can be written into the LIN-UART transmit data register (TDR). Writing data sets the TDRE flag to "0". If transmission is enabled (SCR:TXE = 1) at this time, the data is written to the transmit shift register and the transmission is started sequentially from the start bit in the next serial clock cycle.

When TDRE flag is set to "1" if the transmit interrupt is enabled (TIE = 1), an interrupt is generated when the TDRE flag is set to "1".

When the data length is set to 7-bit (CL = 0), the bit 7 in the TDR is an unused bit regardless of the transfer direction select bit (BDS) setting (LSB-first or MSB-first).

#### Note:

Since the initial value of transmit data empty flag bit (SSR:TDRE) is "1", an interrupt is generated immediately when transmit interrupts are enabled (SSR:TIE =1).

#### Reception

The reception is performed when reception is enabled (SCR:RXE =1). When the start bit is detected, one frame data is received according to the data format defined in the LIN-UART serial control register (SCR). If an error occurs, the error flag (SSR:PE, ORE, FRE) is set. After the reception of the one frame data is completed, the received data is transferred from the reception shift register to the LIN-UART reception data register (RDR), and the reception data register full flag bit (SSR:RDRF) is set to "1". If the reception interrupt request is enabled (SSR:RIE = 1) at this time, a reception interrupt request is output.

To read the received data, check the error flag status and read the received data from the LIN-UART reception data register (RDR) if the reception is normal. If a reception error occurs, perform error handlings.

When the received data is read, the reception data register full flag bit (SSR:RDRF) is cleared to "0".

When the data length is set to 7-bit (CL = 0), the MSB in the TDR is an unused bit regardless of the transfer direction select bit (BDS) setting (LSB-first or MSB-first).

#### Note:

Data in the LIN-UART reception data register (RDR) becomes valid when the reception data register full flag bit (SSR:RDRF) is set to "1" and no error occurs (SSR:PE, ORE, FRE=0).

#### Input clock

Internal or external clock is used. For the baud rate, select the baud rate generator (SMR:EXT = 0 or 1, OTO = 0).

#### Stop bit and reception bus idle flag

You can select one or two stop bits at transmission. When 2-bit of the stop bit are selected, both of the stop bits are detected during reception.

When the first stop bit is detected, the reception data register full flag (SSR:RDRF) is set to "1". When no start bit is detected after that, the reception bus idle flag (ECCR:RBI) is set to "1", indicating that the reception is not performed.

#### Error detection

In mode 0, parity, overrun, and frame errors can be detected.

In mode 1, overrun and frame errors can be detected. But, parity errors cannot be detected.

#### Parity

You can specify whether or not to add (at transmission) and detect (at reception) a parity bit.

The parity enable bit (SCR:PEN) can be used whether or not to use a parity; the parity selection bit (SCR:P) can be used to select the odd or even parity.

In operation mode 1, the parity cannot be used.



#### Figure 22.7-2 Transmission Data when Parity is Enabled

#### Data signaling

NRZ data format.

Data transfer method

The data bit transfer method can be the LSB-first or MSB-first.

# 22.7.2 Operation of Synchronous Mode (Operation Mode 2)

# When LIN-UART is used in operation mode 2 (normal mode), the transfer method is clock synchronous.

#### Operation of Synchronous Mode (Operation Mode 2)

#### Transmit/reception data format

In synchronous mode, you can transmit and receive 8-bit data and select whether or not to include the start bit and stop bit (ECCR:SSM). When the start/stop bit is included (ECCR:SSM = 1), you can select whether or not to include the parity bit (SCR:PEN).

Figure 22.7-3 shows the data format in synchronous mode.

#### Figure 22.7-3 Transmit/Reception Data Format (Operation Mode 2)



Clock inversion function

When the SCES bit in the LIN-UART extended status control register (ESCR) is "1", the serial clock is inverted. In receiving side of serial clock, the LIN-UART samples data at the falling edge of the received serial clock. Note that, in sending side of serial clock, the mark level is set to "0" when the SCES bit is "1".

#### Figure 22.7-4 Transmission Data Format During Clock Inverted



#### Start/stop bit

When the SSM bit in the LIN-UART extended communication control register (ECCR) is "1", the start and stop bits are added to the data format as in asynchronous mode.

#### Clock supply

In clock synchronous mode (normal), the number of the transmit/reception bits must be equal to the number of the clock cycles. When the start/stop bit is enabled, the number of the added start/stop bits must be equal, as well.

When the serial clock output is enabled (SMR:SCKE = 1) in sending side of serial clock (ECCR:MS = 0), a synchronous clock is output automatically at transmission/reception. When the serial clock output is disabled (SMR:SCKE = 0) in receiving side of serial clock (ECCR:MS = 1), the clock for each bit of transmit/reception data must be supplied from the outside.

The clock signal must remain at the mark level ("H") as long as it is irrelevant to transmission/reception.

#### Clock delay

Setting the SCDE bit in the ECCR to "1", a delayed transmit clock is output as shown in Figure 22.7-5. This function is required when the receiving device samples data at the rising or falling edge of the clock.



#### Figure 22.7-5 Transmission Clock Delay (SCDE = 1)

#### Clock inversion

When the SCES bit in the LIN-UART extended status register (ESCR) is "1", the LIN-UART clock is inverted, and received data is sampled at the falling edge of the clock. At this time, the value of the serial data must be enabled at the timing of the clock falling edge.

#### Continuous clock supply

When the CCO bit in the ESCR is "1", the serial clock output from the SCK pin is supplied in the sending side of serial clock continuously. In this mode, add the start/stop bit to the data format (SSM = 1) in order to identify the beginning and end of the data frame. Figure 22.7-6 shows the operation of this function.



#### Figure 22.7-6 Continuous Clock Supply (Mode 2)

#### Error detection

When the start/stop bits are disabled (ECCR:SSM = 0), only overrun errors are detected.

Communication settings for synchronous mode

To communicate in synchronous mode, the following settings are required.

- LIN-UART baud rate generator register (BGR0/BGR1)
  Set the dedicated baud rate reload counter to a required value.
- LIN-UART serial mode register (SMR)

MD1, MD0: "10<sub>B</sub>" (Mode 2)

- SCKE : "1": Use the dedicated baud rate reload counter
  - : "0": Input external clock
- SOE : "1": Enable transmission/reception
  - : "0": Enable reception only
- LIN-UART serial control register (SCR)

RXE, TXE: Set either bit to "1".

- A/D : The value of this bit is disabled so that the address/data format selection function cannot be used.
- CL : This bit is set to 8 bits length automatically, and its value is disabled.

CRE: "1": Since the error flag is cleared, transmission/reception is stopped.

- For SSM = 0:
  - PEN, P, SBL: Since not used, parity bit and stop bit are disabled.
- For SSM = 1:
  - PEN : "1": Add/detect parity bit, "0": Not use parity bit
  - P : "1": Even parity, "0": Odd parity
  - SBL : "1": Stop bit length 2, "0": Stop bit length 1

• LIN-UART serial status register (SSR)

BDS: "0": LSB-first, "1": MSB-first

- RIE : "1": Enable reception interrupt, "0": Disable reception interrupt
- TIE : "1": Enable transmit interrupt, "0": Disable transmit interrupt
- LIN-UART extended communication control register (ECCR)
  - SSM: "0": Not use start/stop bit (normal),
    - "1": Use start/stop bit (extended function),
  - MS : "0": Sending side of serial clock (serial clock output),
    - "1": Receiving side of serial clock (input serial clock from sending side of serial clock)

#### Note:

To start communication, write data into the LIN-UART transmit data register (TDR).

To receive data, disable the serial output (SMR:SOE = 0), and then write dummy data into the TDR. Enabling continuous clock and start/stop bit allows bi-directional communication as in asynchronous mode.

# 22.7.3 Operation of LIN function (Operation Mode 3)

In operation mode 3, the LIN-UART works as the LIN master and the LIN slave. In operation mode 3, the communication format is set to 8-bit data, no parity, stop bit 1, LSB first.

#### Asynchronous LIN Mode Operation

Operation as LIN master

In LIN mode, the master determines the baud rate for the entire bus, and the slave synchronizes to the master.

Writing "1" to the LBR bit in the LIN-UART extended communication control register (ECCR) outputs 13 to 16 bits at the "L" level from the SOT pin. These bits are the LIN synch break signifying the beginning of a LIN message.

The TDRE flag bit in the LIN-UART serial status register (SSR) is set to "0". After the break, it is set to "1" (initial value). If the TIE bit in SSR is "1" at this time, a transmit interrupt is output.

The length of the LIN Synch break transmitted is set by the LBL 0/1 bits in ESCR as in the following table.

Table 22.7-3 LIN Break Length

LBL0	LBL1	Break length
0	0	13 bits
1	0	14 bits
0	1	15 bits
1	1	16 bits

Synch field is transmitted as byte data 0x55 following the LIN break. To prevent generation of a transmit interrupt, 0x55 can be written to the TDR after the LBR bit in ECCR is set to "1" even if the TDRE flag is "0".

#### Operation as LIN slave

In LIN slave mode, the LIN-UART must synchronize to the baud rate for the master. The LIN-UART generates a reception interrupt when LIN break interrupt is enabled (LBIE = 1) even though reception is disabled (RXE = 0). The LBD bit in the ESCR is set to "1" at this time.

Writing "0" to the LBD bit clears the reception interrupt request flag.

For calculation of the baud rate, the following example shows the operation of the LIN-UART. When the LIN-UART detects the first falling edge of Synch field, set an internal signal, which is input to the 8/16-bit compound timer, to "H", and then start the timer. The internal signal should be "L" at the fifth falling edge. The 8/16-bit compound timer must be set to the input capture mode. Also, the 8/16-bit compound timer interrupts must be enabled and set for the detection at both edges. The time for which the input signal to the 8/16-bit compound timer is the value obtained by multiplying the baud rate by 8.

The baud rate setting value is calculated by the following expressions.

When the counter of the 8/16-bit compound timer is not overflowing

: BGR value = (b - a) / 8 - 1

When the counter of the 8/16-bit compound timer is overflowing

: BGR value = (max + b - a) / 8 - 1

max: Maximum value of free-run timer

a: TII0 data register value after the first interrupt

b: TII0 data register value after the second interrupt

Note:

Do not set the baud rate if the new BGR value calculated based on Synch field as above in LIN slave mode involves an error over  $\pm 15\%$ .

For the operations of the input capture function on the 8/16-bit compound timer, see "15.13 Operating Description of Input Capture Function".

LIN synch break detection interrupt and flag

The LIN break detection (LBD) flag in ESCR is set to "1" when the LIN synch break is detected in slave mode. When the LIN break interrupt is enabled (LBIE = 1), an interrupt is generated.



Figure 22.7-7 Timing of LIN Synch Break Detection and Flag Set

The above diagram shows the timing of the LIN synch break detection and flag.

Since the data framing error (FRE) flag bit in SSR generates a reception interrupt two bits earlier than a LIN break interrupt (for communication format is 8-bit data, no parity, "1" stop bit.), set the RXE to "0" when a LIN break is used.

The LIN synch break detection works only in operation mode 3.

Figure 22.7-8 shows the beginning of a typical LIN message and the LIN-UART operation.





• LIN bus timing



Figure 22.7-9 LIN Bus Timing and LIN-UART Signals

### 22.7.4 Serial Pin Direct Access

#### Transmission pin (SOT) or reception pin (SIN) can be accessed directly.

#### LIN-UART Pin Direct Access

The LIN-UART allows the programmer to directly access the serial I/O pins.

The status of the serial input pin (SIN) can be read by using the serial I/O pin direct access bit (ESCR:SIOP).

You can set the value of the serial output pin (SOT) arbitrarily when the serial output is enabled (SMR:SOE=1) after direct write to the serial output pin (SOT) is enabled (ESCR:SOPE = 1), and then "0" or "1" is written to the serial I/O pin direct access bit (ESCR:SIOP).

In LIN mode, this feature is used for reading transmitted data or for error handling when a LIN bus line signal is physically incorrect.

#### Note:

Direct access is allowed only when transmission is not in progress (the transmission shift register is empty).

Before enabling transmission (SMR:SOE = 1), write a value to the serial output pin direct access bit (ESCR:SIOP). This prevents a signal of an unexpected level from being output since the SIOP bit holds a previous value.

While the value of the SIN pin is read by normal read, the value of the SOT pin is read for the SIOP bit by the read-modify-write (RMW) instructions.

# 22.7.5 Bidirectional Communication Function (Normal Mode)

Normal serial bidirectional communication can be performed in operation mode 0 or 2. Asynchronous mode and synchronous mode can be selected in operation modes 0 and 2, respectively.

#### Bidirectional Communication Function

To operate the LIN-UART in normal mode (operation mode 0 or 2), the settings shown in Figure 22.7-10 are required.



#### Figure 22.7-10 Settings of LIN-UART Operation Modes 0 and 2

Inter-CPU connection

For bidirectional communication, interconnect two CPUs as shown in Figure 22.7-11.

#### Figure 22.7-11 Connection Example of Bidirectional Communication in LIN-UART Mode 2



#### • Communication procedure example

The communication is started from transmitting end at arbitrary timing when data is ready to be transmitted. The receiving end returns ANS (per one byte in this example) regularly after the transmitted data is received. Figure 22.7-12 shows an example of bidirectional communication flowchart.





# 22.7.6 Master/Slave Mode Communication Function (Multiprocessor Mode)

Operation mode 1 allows communication between multiple CPUs connected in master/ slave mode. It can be used as a master or slave.

#### Master/Slave Mode Communication Function

To operate the LIN-UART in multiprocessor mode (operation mode 1), the settings shown in Figure 22.7-13 are required.



#### Figure 22.7-13 Settings of LIN-UART Operation Mode 1

Inter-CPU connection

For master/slave mode communication, a communication system is configured by connecting between one master CPU and multiple slave CPUs with two common communication lines, as shown in Figure 22.7-14. The LIN-UART can be used as the master or slave.





#### • Function Selection

For master/slave mode communication, select the operation mode and the data transfer method, as shown in Table 22.7-4.

Table 22.7-4 Select of Master/Slave Mode Communication Function

	Operation mode		Data	Parity	Synchronous	Stop bit	Bit direction
	Master CPU	Slave CPU	Dala	Tanty	method		Dituliection
Address transmission/ reception	Mode 1 (Transmit/	Mode 1 (Transmit/	A/D = 1 + 7-bit or 8-bit address	None	Asunchronous	1 bit or 2 bits	LSB first
Data transmission/ reception	receive A/D bit)	receive A/D bit)	A/D = 0 + 7-bit or 8-bit data	None	Asynchionous		MSB first

#### • Communication procedure

Communication is started by transmitting address data from the master CPU. The address data, whose A/D bit is set as "1", determines the slave CPU to be the destination. Each slave CPU checks address data by using a program, and communicates with the master CPU when the data matches an assigned address.

Figure 22.7-15 shows a flowchart for master/slave mode communication (multiprocessor mode).





# 22.7.7 LIN Communication Function

# For LIN-UART communication, a LIN device can be used in the LIN master system or the LIN slave system.

#### ■ LIN Master/Slave Mode Communication Function

Figure 22.7-16 shows the required settings for the LIN communication mode of LIN-UART (operation mode 3).





• LIN device connection

Figure 22.7-17 shows the communication system between one LIN master and LIN slave.

The LIN-UART can serve as the LIN master or LIN slave.



#### Figure 22.7-17 Example of LIN Bus System Communication

# 22.7.8 Example of LIN-UART LIN Communication Flowchart (Operation Mode 3)

This section shows examples of LIN-UART LIN communication flowchart.

#### ■ LIN Master Device



- If the ESCR:LBD bit is set to "1", execute the LIN-UART reset. Note: Detect an error in each process and handle it appropriately.

Figure 22.7-18 LIN Master Flowchart

#### LIN Slave Device



Figure 22.7-19 LIN Slave Flowchart

\* 2: - If the FRE or ORE flag is set "1", write "1" to the SCR:CRE bit to clear the error flag.

- If the ESCR:LBD bit is set to "1", execute the LIN-UART reset.

Note: Detect an error in each process and handle it appropriately.

### 22.8 Notes on Using LIN-UART

#### This section shows notes on using the LIN-UART.

#### Notes on Using LIN-UART

#### • Enabling operation

The LIN-UART has the TXE (transmission) and RXE (reception) enable bit in the LIN-UART serial control register (SCR) for transmission and reception, respectively. Since both transmission and reception are disabled by default (internal value), these operations must be enabled before transfer. Also, you can disable these operations to stop transfer as required.

#### Setting communication mode

The communication mode must be set while the LIN-UART is stopped. If the mode is set during transmission/reception, the transmitted/received data is not guaranteed.

#### • Timing of enabling transmit interrupts

Since the default (initial) value of the transmit data empty flag bit (SSR:TDRE) is "1" (no transmit data, transmit data write enabled), a transmit interrupt request is generated immediately when transmit interrupt request is enabled (SSR:TIE =1). To prevent this, be sure to set the transmit data before setting the TIE flag to "1".

#### Changing operation setting

Reset the LIN-UART after changing its settings, such as adding the start/stop bit or changing the data format.

The correct operation settings are not guaranteed even if you reset the LIN-UART (SMR:UPCL = 1) concurrently with setting the LIN-UART serial mode register (SMR). Therefore, after setting the bit in LIN-UART serial mode register (SMR), reset the LIN-UART (SMR:UPCL = 1) again.

#### • Using LIN function

Although the LIN functions are available in the operation mode 3, the LIN format is automatically set in the mode 3 (8-bit data, no parity, 1 stop bit, LSB-first).

While the length of LIN break transmit bit is variable, the detection bit length is fixed to 11 bits.

#### • Setting LIN slave

When starting LIN slave mode, be sure to set the baud rate before receiving the LIN synch break in order to make sure that the minimum 13 bits length of the LIN synch break is detected.

#### Bus idle function

The bus idle is not available in synchronous mode 2.

#### A/D bit (LIN-UART serial control register (SCR): Address/data format selection bit)

Be sure to note the followings when using the A/D bit.

The A/D bit is used to select the address/data for transmission when it is written, and to read the A/D bit received last when it reads. Internally, the A/D bit values for transmission and reception are stored in separate registers.

The transmit A/D bit value is read when read-modify-write (RMW) instructions are used. Therefore, an incorrect value may be written to the A/D bit when another bit in the SCR is bit-accessed.

For the above reason, the A/D bit must be set at the last access to the SCR before transmission. Or, the above problem can be prevented by byte-accessing whenever the SCR is written.

#### LIN-UART software reset

Execute the LIN-UART software reset (SMR:UPCL = 1) when the TXE bit in the LIN-UART serial control register (SCR) is "0".

#### Synch break detection

In mode 3 (LIN mode), when serial input has 11 bits width or more and becomes "L", the LBD bit in the extended status control register (ESCR) is set to "1" (Synch break detection) and the LIN-UART waits for the Synch field. As a result, when serial input has more than 11 bits of "0", the LIN-UART recognizes that the Synch break is input (LBD = 1), and then waits for the Synch field.

In this case, execute the LIN-UART reset (SMR: UPCL = 1).

# 22.9 Sample Programs of LIN-UART

#### This section provides sample programs for operating the LIN-UART.

#### ■ Sample Programs of LIN-UART

See the sample programs in "Introduction" for those of the LIN-UART.

#### Setting Procedure Other than Program Examples

• How to select the operation mode

Use the operation mode selection (SMR:MD[1:0]).

	Operation mode	Operation mode selection (MOD[1:0]).
Mode 0	Normal (Asynchronous)	Set to "00 <sub>B</sub> "
Mode 1	Multiprocessor	Set to "01 <sub>B</sub> "
Mode 2	Normal (Synchronous)	Set to "10 <sub>B</sub> "
Mode 3	LIN	Set to "11 <sub>B</sub> "

#### • Operation clock types and how to select it

Use the external clock selection bit (SMR:EXT).

Clock input	External clock selection bit (EXT)
To select a dedicated baud rate generator	Set to "0"
To select an external clock	Set to "1"

#### • How to control the SCK, SIN, and SOT pins

Use the following setting.

	LIN-UART
To set the SCK pin as input	DDR6:P05 =0 SMR:SCKE =0
To set the SCK pin as output	SMR:SCKE =1
To use the SIN pin	DDR6:P07 =0
To use the SOT pin	SMR:SOE =1

#### • How to enable/disable the LIN-UART operation

Use the reception enable bit (SCR:RXE).

Control details	Reception enable bit (RXE)
Disable reception	Set to "0"
Enable reception	Set to "1"

Use the transmit control bit (SCR:TXE).

Control details	Transmit control bit (TXE)
Disable transmission	Set to "0"
Enable transmission	Set to "1"

#### How to use an external clock as the LIN-UART serial clock

Use the one-to-one external clock enable bit (SMR:OTO).

Control details	Reception enable bit (OTO)
Enable external clock	Set to "1"

#### • How to restart the reload counter

Use the reload counter restart bit (SMR:REST).

Control details	Reload counter restart bit (REST)
Restart the reload counter	Set to "1"

#### How to reset the LIN-UART

Use the LIN-UART programmable clear bit (SMR:UPCL).

Control details	LIN-UART programmable clear bit (UPCL)
Reset the LIN-UART software	Set to "1"

#### • How to set the parity

Use the parity enable bit (SCR:PEN) and the parity selection bit (SCR:P).

Operation	Parity control (PEN)	Parity polarity (P)
To set to no parity	Set to "0"	-
To set to even parity	Set to "1"	Set to "0"
To set to odd parity	Set to "1"	Set to "1"

#### • How to set the data length

Use the data length selection bit (SCR:CL).

Operation	Data length selection bit (CL)
To set the bit length to 7	Set to "0"
To set the bit length to 8	Set to "1"

#### • How to select the STOP bit length

Use the STOP bit length control (SCR:SBL).

Operation	STOP bit length control (SBL)
To set STOP bit length to 1	Set to "0"
To set STOP bit length to 2	Set to "1"

#### How to clear the error flag

Use the reception error flag clear bit (SCR:CRE).

Control details	Reception error flag clear bit (CRE)
To clear the error flag (PE, ORE, FRE)	Write "0"

#### How to set the transfer direction

Use the transfer direction selection bit (SSR:BDS).

LSB/MSB can be selected for transfer direction in any operation mode.

Control details	Serial data direction control (BDS)
To select the LSB first (from the least significant bit)	Set to "0"
To select the MSB first (from the most significant bit)	Set to "1"

How to clear the reception completion flag

Uses the following setting.

Control details	Method
To clear the reception completion flag	Read the RDR register

The first RDR register read is the reception initiation.

#### • How to clear the transmit buffer empty flag

Uses the following setting.

Control details	Method
To clear the transmit buffer empty flag	Write to TDR register

The first TDR register write is the transmit initiation.

#### • How to select the data format (Address/Data) (Only in mode 1)

Use the data length selection bit (SCR:A/D).

Operation	Data format selection bit (A/D)
To select the data frame	Set to "0"
To select the address frame	Set to "1"

This is effective only at transmission. The A/D bit is ignored at reception.

#### • How to set the baud rate

See "22.6 LIN-UART Baud Rate".

#### • Interrupt related registers

Interrupt level is set by interrupt level setting registers as in the following table.

	Interrupt level setting register	Interrupt vector
Reception	Interrupt level register (ILR1) Address: 0007A <sub>H</sub>	#7 Address: 0FFFC <sub>H</sub>
Transmission	Interrupt level register (ILR2) Address: 0007B <sub>H</sub>	#8 Address: 0FFEA <sub>H</sub>

• How to enable/disable/clear interrupts

Interrupt request enable flag, interrupt request flag

Interrupt request enable bit (SSR:RIE), (SSR:TIE) is used to enable interrupts.

	UART reception	UART transmission
	Reception interrupt enable bit (RIE)	Reception interrupt enable bit (TIE)
To disable interrupt requests	Set to "0"	
To enable interrupt requests	Set to "1"	

The following setting is used to clear interrupt requests.

	UART reception	UART transmission
To clear interrupt requests	The reception data register full (RDRF) is cleared by reading the LIN-UART serial input register (RDR).	The transmit data register empty (TDRE) is set to "0" by writing data to the LIN-UART serial output data register (TDR).
	The error flags (PE, ORE, FRE) are set to "0" by writing "1" to the error flag clear bit (CRE).	
# CHAPTER 23 8/10-BIT A/D CONVERTER

This chapter describes the functions and operations of the 8/10-bit A/D converter.

- 23.1 Overview of 8/10-bit A/D Converter
- 23.2 Configuration of 8/10-bit A/D Converter
- 23.3 Pins of 8/10-bit A/D Converter
- 23.4 Registers of 8/10-bit A/D Converter
- 23.5 Interrupts of 8/10-bit A/D Converter
- 23.6 Operations of 8/10-bit A/D Converter and Its Setup Procedure Examples
- 23.7 Notes on Use of 8/10-bit A/D Converter
- 23.8 Sample Programs for 8/10-bit A/D Converter

# 23.1 Overview of 8/10-bit A/D Converter

The 8/10-bit A/D converter is a 10-bit successive approximation type of 8/10-bit A/D converter. It can be started via software, external trigger, and internal clock, with one input signal selected from among multiple analog input pins.

#### ■ A/D Conversion Functions

The A/D converter converts analog voltages (input voltages) input to an analog input pin to 10-bit digital values.

- One of multiple analog input pins can be selected.
- The conversion speed is programmable to be configured (selected according to the operating voltage and frequency).
- An interrupt is generated when A/D conversion completes.
- The completion of conversion can also be checked with the ADI bit in the ADC1 register.

To activate A/D conversion functions, follow one of the methods given below.

- Activation using the AD bit in the ADC1 register
- Continuous activation using the external pin (ADTG)
- Continuous activation using the 8/16-bit compound timer output TO00

## 23.2 Configuration of 8/10-bit A/D Converter

The 8/10-bit A/D converter consists of the following blocks:

- Clock selector (input clock selector for starting A/D conversion)
- Analog channel selector
- Sample-and-hold circuit
- Control circuit
- A/D data registers (ADDH, ADDL)
- A/D control register 1 (ADC1)
- A/D control register 2 (ADC2)

#### Block Diagram of 8/10-bit A/D Converter

Figure 23.2-1 is a block diagram of the 8/10-bit A/D converter.



#### Figure 23.2-1 Block Diagram of 8/10-bit A/D Converter

#### Clock selector

This block selects the A/D conversion clock with continuous activation enabled (ADC2:EXT = 1).

#### Analog channel selector

This circuit selects one of multiple analog input pins.

#### Sample-and-hold circuit

This circuit holds the input voltage selected by the analog channel selector. This enables A/D conversion to be performed without being affected by variation in input voltage during conversion (comparison) by sampling and holding the input voltage immediately after starting A/D conversion.

#### • Control circuit

The A/D conversion function determines the values in the 10-bit A/D data register sequentially from MSB to LSB based on the voltage compare signals from the comparator. When conversion is completed, the A/D conversion function sets the interrupt request flag bit (ADC1: ADI).

#### A/D data registers (ADDH/ADDL)

The high-order two bits of 10-bit A/D data are stored in the ADDH register; the low-order eight bits are stored in the ADDL register.

Setting the A/D conversion precision bit (ADC2:AD8) to "1" provides 8-bit precision, storing the upper eight bits of the 10-bit A/D data in the ADDL register.

#### A/D control register 1 (ADC1)

This register is used to enable and disable functions, select an analog input pin, check statuses, and control interrupts.

#### A/D control register 2 (ADC2)

This register is used to select an input clock, enable and disable interrupts, and select functions.

#### Input Clock

The 8/10-bit A/D converter uses the output clock from the prescaler as the input clock (operation clock).

### 23.3 Pins of 8/10-bit A/D Converter

#### This section describes the pins of the 8/10-bit A/D converter.

#### Pins of 8/10-bit A/D Converter

MB95130/M series has 8 channels of analog input pin. Analog input pins also serve as general-purpose I/O ports.

#### AN07 to AN00 Pin

- AN07 to AN00: When using the A/D conversion function, input the analog voltage you wish to convert to one of these pins. Each of the pins serves as an analog input pin by selecting it using the analog input channel select bits (ADC1: ANS0 to ANS3) with the corresponding bit in the port direction register (DDR) set to 0. Even when the 8/10-bit A/D converter is used, the pins not used for analog input can be used as general-purpose I/O ports. Note that the number of analog input pins differs depending on the series.
- ADTG Pin

ADTG: This is a pin used to activate A/D conversion function by external trigger.

AV<sub>CC</sub> pin

AV<sub>CC</sub>:

This is a 8/10-bit A/D converter power supply pin. Use this at the same potential as  $V_{CC}$ . If A/D conversion precision is demanded, you should take measures to ensure that  $V_{CC}$  noise does not enter AV<sub>CC</sub>, or use a separate power source. You should connect this pin to a power source even when the 8/10-bit A/D converter is not being used.

#### • AV<sub>SS</sub> pin

AV<sub>SS</sub>: This is a ground pin of the 8/10-bit A/D converter. Use this at the same potential as  $V_{SS}$ . When A/D conversion precision is required, take measures to ensure that the  $V_{SS}$  noise does not interfere with AV<sub>SS</sub>. You should connect this pin to a ground (GND) even when the 8/10-bit A/D converter is not being used.



#### ■ Block Diagram of Pins Related to 8/10-bit A/D Converter

# 23.4 Registers of 8/10-bit A/D Converter

# The 8/10-bit A/D converter has four registers: A/D control register 1 (ADC1), A/D control register 2 (ADC2), A/D data register H (ADDH), and A/D data register L (ADDL).

#### ■ List of 8/10-bit A/D Converter Registers

Figure 23.4-1 lists the registers of the 8/10-bit A/D converter.

		i iguic z		gisters					
8/10-bit A/D converter control register 1 (ADC1)									
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
006C <sub>H</sub>	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	ADMVX	AD	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R(RM1),W	R/WX	R/W	R0,W	
8/10-bit A/D c	converter cor	ntrol regist	er 2 (ADC	2)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
006D <sub>H</sub>	AD8	TIM1	TIM0	ADCK	ADIE	EXT	CKDIV1	CKDIV0	00000000 <sub>B</sub>
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
8/10-bit A/D c	converter dat	a register	H (ADDH	)					
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
006E <sub>H</sub>	-	-	-	-	-	-	SAR9	SAR8	00000000 <sub>B</sub>
	R0/WX	R0/WX	R0/WX	R0/WX	R0/WX	R0/WX	R/WX	R/WX	
8/10-bit A/D c	converter dat	a register	L (ADDL)						
Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
006F <sub>H</sub>	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	SAR0	00000000 <sub>B</sub>
	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	
<ul> <li>R/W: Readable/writable (Read value is the same as write value)</li> <li>R0, W: Write only (Writable, "0" is read)</li> <li>R/WX: Read only (Readable, writing has no effect on operation)</li> <li>R0/WX: Undefined bit (Read value is "0", writing has no effect on operation)</li> <li>R(RM1), W: Readable/writable (Read value is different from write value, "1" is read by read-modify-write (RMW) instruction)</li> </ul>									

#### Figure 23.4-1 Registers of 8/10-bit A/D Converter

■ 8/10-bit A/D Converter Control Register 1 (ADC1)

# 23.4.1 8/10-bit A/D Converter Control Register 1 (ADC1)

8/10-bit A/D converter control register 1 (ADC1) is used to enable and disable individual functions of the 8/10-bit A/D converter, select an analog input pin, and to check the states.

#### Figure 23.4-2 8/10-bit A/D Converter Control Register 1 (ADC1) Address bit7 bit6 bit5 bit4 bit3 bit2 bit1 bit0 Initial value ANS1 ANS3 ANS2 ANS0 ADMVX 0000000в 006Сн ADI ADMV AD R/W R/W R/W R(RM1),WR/WX R/W R/W R0,W AD A/D conversion start bit 0 Do not start A/D conversion. 1 Start A/D conversion. ADMVX Current cut-off analog switch control bit 0 Turn on analog switch only during conversion. 1 Maintain analog switch on. ADMV Conversion flag bit 0 Not converting Currently converting 1 Interrupt request flag bit ADI Read Write 0 Conversion not completed Clear this bit. Conversion completed Make no changes to the bit 1 with no effect on others. ANS2 ANS1 ANS0 Analog input channel select bits ANS3 0 0 0 0 AN00 pin 0 0 0 1 AN01 pin 0 0 1 0 AN02 pin 0 0 1 1 AN03 pin 0 1 0 0 AN04 pin 0 1 0 1 AN05 pin 0 0 1 1 AN06 pin 0 1 1 1 AN07 pin R/W : Readable/writable (Read value is the same as write value) R/WX : Read only (Readable, writing has no effect on operation) : Write only (Writable, "0" is read) R0,W R(RM1),W : Readable/writable (Read value is different from write value, "1" is read by read-modify-write (RMW) instruction) : Initial value Γ

Do not select the unusable channel for the MB95130/M series by analog input channel select bits.

Bit name		Function
bit7 bit6 bit5 bit4	ANS3, ANS2, ANS1, ANS0: Analog input channel select bits	<ul> <li>Select the analog input pin to be used from among AN00 to AN07.</li> <li>Note that the number of analog input pins differs depending on the series.</li> <li>When A/D conversion is activated (AD = 1) via software (ADC2: EXT = 0), these bits can be updated at the same time.</li> <li>Note: When the ADMV bit is "1", do not update these bits. The pins not used as analog input pins can be used as general-purpose ports.</li> </ul>
bit3	ADI: Interrupt request flag bit	<ul> <li>Detects the termination of A/D conversion.</li> <li>When the A/D conversion function is used, the bit is set "1" upon termination of A/D conversion.</li> <li>Interrupt requests are output when this bit and the interrupt request enable bit (ADC2: ADIE) are both "1".</li> <li>When written to this bit, "0" clears it; "1" leaves it unchanged with no affect on others.</li> <li>When read by a read-modify-write (RMW) instruction, the bit returns "1".</li> </ul>
bit2	ADMV: Conversion flag bit	Indicates that conversion is ongoing during execution of the A/D conversion function. The bit contains "1" during conversion. This bit is read-only. Any value attempted to be written is meaningless and has no effect on operation.
bit1	ADMVX: Analog switch for shutting down control bit	Controls the analog switch for shutting down the internal reference power supply. When the external impedance of the AVR pin is high, rush current flows immediately after A/D startup and may affect A/D conversion precision. In this kind of situation, this can be avoided by setting this bit to "1" before A/D startup. Set the bit to "0" before switching to standby mode, in order to reduce current consumption. Note that some series do not have AVR pins, and are internally connected to AV <sub>CC</sub> .
bit0	AD: A/D conversion startup bit	<ul> <li>Starts the A/D conversion function via software.</li> <li>Writing "1" to the bit starts the A/D conversion function.</li> <li>Note: Writing "0" to this bit will not stop operation of the A/D conversion function. The value read is always "0".</li> <li>A/D conversion startup by this bit is disabled with EXT=1.</li> <li>A/D converter re-starts by writing "1" to this bit during A/D conversion with EXT = 0.</li> </ul>

Table 23.4-1 Functions of Bits in 8/10-bit A/D Converter Control Register 1 (ADC1)

# 23.4.2 8/10-bit A/D Converter Control Register 2 (ADC2)

8/10-bit A/D converter control register 2 (ADC2) selects the 8/10-bit A/D converter function, selects the input clock, and performs interrupt and status checking.

#### ■ 8/10-bit A/D Converter Control Register 2 (ADC2)





Bit name		Function
bit7	AD8: Precision select bit	<ul> <li>This bit selects the resolution of A/D conversion.</li> <li>When set to "0": The bit selects 10-bit precision.</li> <li>When set to "1": The bit selects 8-bit precision, in which case eight bits of data can be read from the ADDL register.</li> <li>Note: The data bits used are different depending on the resolution.</li> <li>Update this bit only with A/D operation stopped before starting conversion.</li> </ul>
bit6 bit5	TIM1, TIM0: Sampling time select bits	<ul> <li>Set the sampling time.</li> <li>Change this sampling time setting depending on the operating conditions (voltage and frequency).</li> <li>The CKIN value is determined by the clock select bits (ADC2:CKDIV1, DKDIV0).</li> <li>Note: Update this bit only with A/D operation stopped.</li> </ul>
bit4	ADCK: External start signal select bit	Selects the start signal for external start (ADC2:EXT = 1).
bit3	ADIE: Interrupt request enable bit	<ul><li>Enables or disables output of interrupts to the interrupt controller.</li><li>Interrupt requests are output with both of this bit and the interrupt request flag bit (ADC1: ADI) set to "1".</li></ul>
bit2	EXT: Continuous activation enable bit	• Selects whether to activate the A/D conversion function via software, or continuously upon detection of the rise of the input clock signal.
bit1 bit0	CKDIV1, CKDIV0: Clock select bits	<ul> <li>Select the clock to use for A/D conversion. The input clock is generated by the prescaler. See "CHAPTER 6 CLOCK CONTROLLER" for details.</li> <li>The sampling time can also be changed via this clock selection.</li> <li>Change this setting depending on the operating conditions (voltage and frequency). Note: Update this bit only with A/D operation stopped.</li> </ul>

Table 23.4-2 Functions of Bits in 8/10-bit A/D Converter Control Register 2 (ADC2)

# 23.4.3 8/10-bit A/D Converter Data Registers Upper/Lower (ADDH, ADDL)

The 8/10-bit A/D converter data registers upper/lower (ADDH, ADDL) contain the results of 10-bit A/D conversion.

The high-order two bits of 10-bit data correspond to the ADDH register; the low-order eight bits correspond to the ADDL register.

#### ■ 8/10-bit A/D Converter Data Registers Upper/Lower (ADDH, ADDL)

ADDH Address	Dit7	Dit6 -	Dit5 -	Dit4 -	Dit3	Dit2	Dit1 SAR9	SAR8	Initial value 00000000 <sub>B</sub>
006E <sub>H</sub>	R0/WX	R0/WX	R0/WX	R0/WX	R0/WX	R0/WX	R/WX	R/WX	
ADDL	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	Initial value
Address	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	SAR0	00000000 <sub>B</sub>
006Fu	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	

Figure 23.4-4 8/10-bit A/D Converter Data Registers Upper/Lower (ADDH, ADDL)

The upper two bits of 10-bit A/D data correspond to bits "1" and "0" in the ADDH register; the lower eight bits correspond to bits 7 to 0 in the ADDL register.

Set the AD8 bit in the ADC2 register to "1" to select 8-bit precision mode, so that 8-bit data can be read from the ADDL register.

These registers are read-only. Writing either is meaningless.

During 8-bit conversion, SAR8 and SAR9 hold "0".

#### • A/D conversion functions

When A/D conversion is started, the results of conversion are finalized and stored in these registers after the conversion time according to the register settings has passed. After A/D conversion finishes, therefore, read the A/D data registers (conversion results), write "0" to the ADI bit (bit 3) in the ADC1 register before the next A/D conversion terminates, then after A/D conversion finishes, clear the flag. During A/D conversion, the registers contain the values resulting from the last conversion performed.

# 23.5 Interrupts of 8/10-bit A/D Converter

# An interrupt source of the 8/10-bit A/D converter is Completion of conversion when A/D conversion functions are operating.

#### ■ Interrupts During 8/10-bit A/D Converter Operation

When A/D conversion is completed, the interrupt request flag bit (ADC1: ADI) is set to "1". Then if the interrupt request enable bit is enabled (ADC2: ADIE = 1), an interrupt request is issued to the interrupt controller. Write "0" to the ADI bit using the interrupt service routine to clear the interrupt request.

The ADI bit is set when A/D conversion is completed, irrespective of the value of the ADIE bit.

The CPU cannot return from interrupt processing if the interrupt request flag bit (ADC1: ADI) is 1 with interrupt requests enabled (ADC2: ADIE = 1). Be sure to clear the ADI bit within the interrupt service routine.

#### Register and Vector Table Related to 8/10-bit A/D Converter Interrupts

#### Table 23.5-1 Register and Vector Table Related to 8/10-bit A/D Converter Interrupts

Interrupt Source	Interrupt Request	Interrupt Le Reg	evel Setting ister	Vector Table Address		
	No.	Register	Setting bit	Upper	Lower	
8/10-bit A/D	IRQ18	ILR4	L18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	

Refer to "APPENDIX B Table of Interrupt Causes" for the interrupt request numbers and vector tables of all peripheral resources are covered in.

# 23.6 Operations of 8/10-bit A/D Converter and Its Setup Procedure Examples

# The EXT bit in the ADC1 register can be used to select the software activation or continuous activation of the 8/10-bit A/D converter.

#### ■ Operations of 8/10-bit A/D Converter's Conversion Function

Software activation

The settings shown in Figure 23.6-1 are required for software activation of the A/D conversion function.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC1	ANS3	ANS2	ANS1	ANS0	ADI	ADMV	ADMVX	AD
	0	0	0	0	0	0	0	1
ADC2	AD8	TIM1	TIMO	ADCK	ADIE	EXT	CKDIV1	CKDIV0
-	0	0	0	×	0	0	0	0
ADDH	-	-	-	-	-	-	A/D converted v	alue retained
ADDL			A/D co	onverted v	alue is ret	tained.		
○ · Pit used								
⊚. Bit used x: Bit unused								
1: Set to "1"								
0: Set to "0"								

#### Figure 23.6-1 Settings for A/D Conversion Function (Software Activation)

When A/D conversion is activated, the A/D conversion function starts working. In addition, even during conversion, the A/D conversion function can be reactivated.

#### Continuous activation

The settings shown in Figure 23.6-2 are required for continuous activation of the A/D conversion function.



#### Figure 23.6-2 Settings for A/D Conversion Function (Continuous Activation)

When continuous activation is enabled, A/D conversion is activated at the rising edge of the selected input clock to start the A/D conversion function. Continuous activation is stopped by disabling it (ADC2:EXT = 0).

#### Operations of A/D Conversion Function

This section details the operations of the 8/10-bit A/D converter.

- 1) When A/D conversion is started, the conversion flag bit is set (ADC1:ADMV = 1) and the selected analog input pin is connected to the sample-and-hold circuit.
- 2) The voltage at the analog input pin is loaded into the sample-and-hold capacitor in the sample-and-hold circuit during the sampling cycle. This voltage is held until A/D conversion has been completed.
- 3) The comparator in the control circuit compares the voltage loaded into the sample-and-hold capacitor with the A/D conversion reference voltage, from the most significant bit (MSB) to the least significant bit (LSB), and then sends the results to the ADDH and ADDL registers.

After the results have been completely transferred, the conversion flag bit is cleared (ADC1:ADMV = 0) and the interrupt request flag bit is set (ADC1:ADI = 1).

Notes:

- When the A/D conversion function is used, the contents of the ADDH and ADDL registers are retained upon completion of A/D conversion. During A/D conversion, the values resulting from the last conversion are loaded.
- Do not re-select the analog input channel (ADC1: ANS3 to ANS0) while the AD conversion function is running, in particular, during continuous activation. Disable continuous activation (ADC2: EXT = 0) before re-selecting the analog input channel.
- Starting the reset, stop, or watch mode stops the 8/10-bit A/D converter and initializes each register.

#### Setup Procedure Example

Follow the procedure below to set up the 8/10-bit A/D converter:

- Initialization
  - 1) Set the port for input (DDR1).
  - 2) Set the interrupt level (ILR4).
  - 3) Enable A/D input (ADC1:ANS0 to ANS3).
  - 4) Set the sampling time (ADC2:TIM1, TIM0).
  - 5) Select the clock (ADC2:CKDIV1, CKDIV0).
  - 6) Set A/D conversion properties (ADC2:AD8).
  - 7) Select the operation mode (ADC2:EXT).
  - 8) Select the startup trigger (ADC2:ADCK).
  - 9) Enable interrupts (ADC2:ADIE=1).
  - 10)Activate A/D (ADC1:AD=1).

#### Interrupt processing

- 1) Clear the interrupt request flag (ADC1:ADI=0).
- 2) Read converted values (ADDH, ADDL).
- 3) Activate A/D (ADC1:AD=1).

### 23.7 Notes on Use of 8/10-bit A/D Converter

#### This section summarizes notes on using the 8/10-bit A/D converter.

#### ■ Notes on Use of 8/10-bit A/D Converter

- Notes on programmed setup
  - When the A/D conversion function is used, the contents of the ADDH and ADDL registers are retained upon completion of A/D conversion. During A/D conversion, the values resulting from the last conversion are loaded.
  - Do not re-select the analog input channel (ADC1: ANS3 to ANS0) while the A/D conversion function is running, in particular, during continuous activation. Disable continuous activation (ADC2: EXT = 0) before re-selecting the analog input channel.
  - Starting the reset, stop, or watch mode stops the 8/10-bit A/D converter and initializes each register.
  - The CPU cannot return from interrupt processing if the interrupt request flag bit (ADC1: ADI) is 1 with interrupt requests enabled (ADC2: ADIE = 1). Be sure to clear the ADI bit within the interrupt service routine.

#### Note on interrupt requests

If A/D conversion is reactivated (ADC1: AD = 1) and terminated at the same time, the interrupt request flag bit (ADC1: ADI) is set.

• Error

As |AVR-AV<sub>SS</sub>| decreases, an error increases relatively.

8/10-bit A/D converter and analog input power-on/shut-down sequences

Turn on the 8/10-bit A/D converter power supply  $(AV_{CC}, AV_{SS})$  and analog input (AN00 to AN07) at the same as or after turning on the digital power supply  $(V_{CC})$ .

In addition, turn off the digital power supply ( $V_{CC}$ ) either at the same time as or after turning off the 8/10bit A/D converter power supply ( $AV_{CC}$ ,  $AV_{SS}$ ) and analog input (AN00 to AN07).

Be careful not to let the  $AV_{CC}$ ,  $AV_{SS}$ , and analog input exceed the voltage of the digital power supply when turning the 8/10-bit A/D converter on and off.

#### Conversion time

The conversion speed of the A/D conversion function is affected by the clock mode, main clock oscillation frequency, and main clock speed switching (gear function).

Example: Sampling time = CKIN × (ADC2: TIM1/TIM0 setting)

Compare time = CKIN x 10 (fixed value) + MCLK

Conversion time = A/D start processing time + sampling time + compare time

- The error max. 1CKIN-1MCLK may occur depending on the timing of A/D startup.
- Program the software satisfied with "sampling time" and "compare time" in A/D conversion of data sheet.

### 23.8 Sample Programs for 8/10-bit A/D Converter

#### Fujitsu provides sample programs to operate the 8/10-bit A/D converter.

#### ■ Sample Programs for 8/10-bit A/D Converter

For sample programs for the 8/10-bit A/D converter, see " Sample Programs" in "Preface".

#### Setting Methods not Covered by Sample Programs

• Selecting the operating clock for the 8/10-bit A/D converter

Use the clock select bits (ADC2:CKDIV1/CKDIV0) to select the operating clock.

• Selecting the sampling time of the 8/10-bit A/D converter

Use the sampling time select bits (ADC2:TIM1/TIM0) to select the sampling time.

• Controlling the analog switch for internal reference power shutdown of the 8/10-bit A/D converter

Use the analog switch control bit (ADC1:ADMVX) to control the internal reference power shutdown analog switch.

Control item	Analog switch control bit (ADMVX)
To turn off internal reference power supply	Set the bit to "0".
To turn on internal reference power supply	Set the bit to "1".

• Selecting the 8/10-bit A/D converter activation method

Use the continuous activation enable bit (ADC2:EXT) to select the startup trigger.

A/D startup factor	Continuous activation enable bit (EXT)
To select the software trigger	Set the bit to "0".
To select the input clock rising signal	Set the bit to "1".

• Generating a software trigger

Use the A/D conversion start bit (ADC1:AD) to generate a software trigger.

Operation	A/D conversion start bit (AD)
To generate a software trigger	Set the bit to "1".

#### • Activation using the input clock

A startup trigger is generated at the rise of the input clock signal.

To select the input clock, use the external start signal select bit (ADC2:ADCK).

Input clock	External start signal select bit (ADCK)
To select the ADTG input pin	Set the bit to "0".
To select the 8/16-bit compound timer (TDO0)	Set the bit to "1".

#### • Selecting the A/D conversion precision

To select the precision of conversion results, use the precision select bit (ADC2:AD8).

Operating mode	Precision select bit (AD8)
To select 10-bit precision	Set the bit to "0".
To select 8-bit precision	Set the bit to "1".

#### • Using analog input pins

To select an analog input pin, use the analog input channel select bits (ADC1:ANS3 to ANS0).

Operation	Analog input channel select bits (ANS3 to ANS0)
To use the AN0 pin	Set the pins to "0000 <sub>B</sub> ".
To use the AN1 pin	Set the pins to "0001 <sub>B</sub> ".
To use the AN2 pin	Set the pins to "0010 <sub>B</sub> ".
To use the AN3 pin	Set the pins to "0011 <sub>B</sub> ".
To use the AN4 pin	Set the pins to "0100 <sub>B</sub> ".
To use the AN5 pin	Set the pins to "0101 <sub>B</sub> ".
To use the AN6 pin	Set the pins to "0110 <sub>B</sub> ".
To use the AN7 pin	Set the pins to "01111 <sub>B</sub> ".

#### • Checking the completion of conversion

The following two methods can be used to check whether conversion has been completed.

• Checking with the interrupt request flag bit (ADC1:ADI)

Interrupt request flag bit (ADI)	Meaning
The value read is "0".	A/D conversion completed with no interrupt request
The value read is "1".	A/D conversion completed with interrupt request generated

• Checking with the conversion flag bit (ADC1:ADMV)

Conversion flag bit (ADMV)	Setting
The value read is "0".	A/D conversion completed (suspended)
The value read is "1".	A/D conversion in progress

#### Interrupted related register

Use the following interrupt level setting register to set the interrupt level.

Interrupt source	Interrupt level setting register	Interrupt vector
8/10-bit AD	Interrupt level register (ILR4) Address: 0007D <sub>H</sub>	#18 Address: 0FFD6 <sub>H</sub>

#### • Enabling, disabling, and clearing interrupts

To enable interrupts, use the interrupt request enable bit (ADC2:ADIE).

Control item	Interrupt request enable bit (ADIE)
To disable interrupt requests	Set the bit to "0".
To enable interrupt requests	Set the bit to "1".

To clear interrupt requests, use the interrupt request bit (ADC1:ADI).

Control item	Interrupt request bit (ADI)
To clear an interrupt request	Set the bit to "1" or activate A/D.

# CHAPTER 24 LOW-VOLTAGE DETECTION RESET CIRCUIT

This chapter describes the functions and operations of the low-voltage detection reset circuit.

- 24.1 Overview of Low-voltage Detection Reset Circuit
- 24.2 Configuration of Low-voltage Detection Reset Circuit
- 24.3 Pins of Low-voltage Detection Reset Circuit
- 24.4 Operations of Low-voltage Detection Reset Circuit

### 24.1 Overview of Low-voltage Detection Reset Circuit

The low-voltage detection reset circuit monitors the power supply voltage and generates a reset signal if the voltage drops below the detection voltage level (available as an option to 5-V products only).

#### ■ Low-voltage Detection Reset Circuit

This circuit monitors the power supply voltage and generates a reset signal if the voltage drops below the detection voltage level. The circuit can be selected as an option to 5-V products only. Refer to the data sheet for details of the electrical characteristics.

# 24.2 Configuration of Low-voltage Detection Reset Circuit

Figure 24.2-1 is a block diagram of the low-voltage detection reset circuit.

#### ■ Block Diagram of Low-voltage Detection Reset Circuit



# 24.3 Pins of Low-voltage Detection Reset Circuit

#### This section explains the pins of the low-voltage detection reset circuit.

#### ■ Pins Related to Low-voltage Detection Reset Circuit

• V<sub>CC</sub> pin

The low-voltage detection reset circuit monitors the voltage at this pin.

V<sub>SS</sub> pin

This pin is a GND pin serving as the reference for voltage detection.

#### • RST pins

The low-voltage detection reset signal is output inside the microcontroller and to this pin.

# 24.4 Operations of Low-voltage Detection Reset Circuit

# The low-voltage detection reset circuit generates a reset signal if the power supply voltage falls below the detection voltage.

#### Operations of Low-voltage Detection Reset Circuit

The low-voltage detection reset circuit generates a reset signal if the power supply voltage falls below the detection voltage. If the voltage is subsequently detected to have recovered, the circuit outputs a reset signal for the duration of the oscillation stabilization wait time to cancel the reset.

For details on the electrical characteristics, see the data sheet.





#### Operations in Standby Mode

The low-voltage detection reset circuit remains operating even in standby modes (stop, sleep, sub clock, and watch modes).

# CHAPTER 25 256-KBIT FLASH MEMORY

This chapter describes the functions and operations of 256-Kbit flash memory.

- 25.1 Overview of 256-Kbit Flash Memory
- 25.2 Sector Configuration of Flash Memory
- 25.3 Register of Flash Memory
- 25.4 Starting the Flash Memory Automatic Algorithm
- 25.5 Checking the Automatic Algorithm Execution Status
- 25.6 Details of Programming/Erasing Flash Memory
- 25.7 Features of Flash Security

## 25.1 Overview of 256-Kbit Flash Memory

The following methods can be used to program (write) and erase data into/from flash memory:

- Programming/erasing using a parallel programmer
- Programming/erasing using a dedicated serial programmer
- Programming/erasing by program execution

This section describes "programming/erasing by program execution".

#### Overview of 256-Kbit Flash Memory

256-Kbit flash memory is located from  $8000_{\rm H}$  to  $\rm FFFF_{\rm H}$  on the CPU memory map. The function of the flash memory interface circuit provides read access and program access from the CPU to flash memory.

As flash memory can be programmed and erased by the instructions from the CPU via the flash memory interface circuit, you can efficiently reprogram (update) program code and data in flash memory with the device mounted on a circuit board.

#### ■ Features of 256-Kbit Flash Memory

- Sector configuration: 32K bytes  $\times 8$  bits
- Automatic program algorithm (Embedded Algorithm)
- Detection of completion of programming/erasing using the data polling or toggle bit function
- Detection of completion of programming/erasing by CPU interrupts
- Compatible with JEDEC standard command
- Programming/erase count (minimum): 10,000 times

#### Programming and Erasing Flash Memory

- It is not possible to write to and read from the flash memory at the same time.
- To program/erase data into/from a bank in flash memory, execute the one copied from the flash memory to RAM, so that writing to the flash memory can be performed.

# 25.2 Sector Configuration of Flash Memory

#### This section explains the registers and the sector configuration of flash memory.

#### Sector Configuration of 256-Kbit Flash Memory

Figure 25.2-1 shows the sector configuration of the 256-Kbit flash memory. The upper and lower addresses of each sector are given in the figure.

Figure 25.2-1	Sector Configuration of 256-Kbit Flash Memory	,
i iguio zoiz i	coold configuration of 200 hold hadring	/

FLASH memory	CPU address	Programmer address*	
32 Kbytes	8000 <sub>H</sub>	18000 <sub>H</sub>	
	F <u>F</u> FF <sub>H</sub>	1 <u>FFFF<sub>H</sub></u>	
*: Programmer addres programs data into These programmer	sses are correspondir flash memory. addresses are used fo	ng to CPU addresses, used or the parallel programmer to	when the parallel programmer program or erase data in flash memory.

# 25.3 Register of Flash Memory

#### This section shows the register of the flash memory

#### ■ Register of the Flash Memory

0072 <sub>H</sub> -       RDYIRQ       RDY       Reserved       IRQEN       WRE       Reserved       000X0         R0/WX       R0/WX       R(RM1),W       R/WX       R/W0       R/W       R/W0       000X0         R/W:       Readable/writable (Read value is the same as write value)       R(RM1),W:       Readable/writable (Read value is different from write value, "1" is read by read-modify-write	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value
R0/WX       R0/WX       R(RM1),w       R/WX       R/W0       R/W       R/W0         R/W:       Readable/writable (Read value is the same as write value)       R(RM1), W:       Readable/writable (Read value is different from write value, "1" is read by read-modify-w	0072 <sub>H</sub>	-	-	RDYIRQ	RDY	Reserved	IRQEN	WRE	Reserved	000X0000 <sub>E</sub>
R/W:Readable/writable (Read value is the same as write value)R(RM1), W:Readable/writable (Read value is different from write value, "1" is read by read-modify-w		R0/WX	R0/WX	R(RM1),W	R/WX	R/W0	R/W	R/W	R/W0	
instruction)		Readable/writable (Read value is different from write value, "1" is read by read-modify-write								
R/WX: Read only (Readable, writing has no effect on operation)	RM1), W: F	Readable/wi	ritable (Re	ead value i	is differen	nt from writ	te value, "	1" is read	by read-m	odify-write
R/W0: Reserved bit (Write value is "0", read value is the same as write value)	RM1), W: F i /X: F	Readable/w nstruction) Read only (F	ritable (R∉ Readable,	ead value i writing ha	is differen 1s no effe	it from writ ct on oper	te value, "' ation)	1" is read	by read-m	odify-write

#### Figure 25.3-1 Register of the Flash Memory

# 25.3.1 Flash Memory Status Register (FSR)

#### Figure 25.3-2 lists the functions of the flash memory status register (FSR).

#### ■ Flash Memory Status Register (FSR)



#### Table 25.3-1 Functions of Flash Memory Status Register (FSR)

	Bit name	Function
bit7 bit6	-: Undefined bits	The value read is always "0". Writing has no effect on the operation.
bit5	RDYIRQ: Flash memory operation flag bit	<ul> <li>This bit shows the operating state of flash memory.</li> <li>The RDYIRQ bit is set to "1" upon completion of the flash memory automatic algorithm when flash memory programming/erasing is completed.</li> <li>An interrupt request occurs when the RDYIRQ bit is set to "1" if interrupts triggered by the completion of flash memory programming/erasing have been enabled (FSR:IRQEN = 1).</li> <li>If the RDYIRQ bit is set to "0" when flash memory programming/erasing is completed, further flash memory programming/erasing is disabled.</li> <li>Setting the bit to "0": Clears the bit.</li> <li>Setting the bit to "1": Has no effect on the operation.</li> <li>"1" is read from the bit whenever a read-modify-write (RMW) instruction is used.</li> </ul>
bit4	RDY: Flash memory program/erase status bit	<ul> <li>This bit shows the programming/erasing status of flash memory.</li> <li>Flash memory programming/erasing cannot be performed with the RDY bit set to "0".</li> <li>A read/reset command can be accepted even when the RDY bit contains "0". The RDY bit is set to "1" upon completion of programming/erasing.</li> <li>It takes a delay of two machine clock (MCLK) cycles after the issuance of a program/erase command for the RDY bit to be set to "0". Read this bit after, for example, inserting NOP twice after issuing the program/erase command.</li> </ul>
bit3	Reserved: Reserved bit	Be sure to set this bit to "0".
bit2	IRQEN: Flash memory program/erase interrupt enable bit	<ul> <li>This bit enables or disables the generation of interrupt requests in response to the completion of flash memory programming/erasing.</li> <li>Setting the bit to "1": Causes an interrupt request to occur when the flash memory operation flag bit is set to "1" (FSR:RDYIRQ = 1).</li> <li>Setting the bit to "0": Prevents an interrupt request from occurring even when the flash memory operation flag bit is set to "1" (FSR:RDYIRQ = 1).</li> </ul>
bit1	WRE: Flash memory program/erase enable bit	<ul> <li>This bit enables or disables the programming/erasing of data into/from the flash memory area. Set the WRE bit before invoking a flash memory program/erase command.</li> <li>Setting the bit to "0": Prevents a program/erase signal from being generated even when a program/erase command is input.</li> <li>Setting the bit to "1": Allows flash memory programming/erasing to be performed after a program/erase command is input.</li> <li>When flash memory is not to be programmed or erased, set the WRE bit to "0" to prevent it from being accidentally programmed or erased.</li> <li>To program data into the flash memory, set FSR:WRE to "1" to write-enable the flash memory and set the flash memory sector write control register (SWRE0/SWRE1). When FSR:WRE disables programming (contains "0"), write access to flash memory does not take place even though it is enabled by the flash memory write control register (SWRE0/SWRE1).</li> </ul>
bit0	Reserved: Reserved bit	Be sure to set this bit to "0".

# 25.4 Starting the Flash Memory Automatic Algorithm

# There are three types of commands that invoke the flash memory automatic algorithm: read/reset, write (program), and chip-erase.

#### Command Sequence Table

Table 25.4-1 lists the commands used in programming/erasing flash memory.

Table 25.4-1 :Command Sequence

Command Bus write		1st bus write cycle		2nd bus write cycle		3rd bus write cycle		4th bus write cycle		5th bus write cycle		6th bus write cycle	
sequence cycle	cycle	Address	Data	Address	Data								
Bood/recet*	1	$F_X X X_H$	F0 <sub>H</sub>	-	-	-	-	-	-	-	-	-	-
Read/reset*	4	UAAA <sub>H</sub>	AA <sub>H</sub>	U554 <sub>H</sub>	55 <sub>H</sub>	UAAA <sub>H</sub>	F0 <sub>H</sub>	RA	RD	-	-	-	-
Write	4	UAAA <sub>H</sub>	AA <sub>H</sub>	U554 <sub>H</sub>	55 <sub>H</sub>	UAAA <sub>H</sub>	$A0_{\rm H}$	PA	PD	-	-	-	-
Chip erase	6	XAAA <sub>H</sub>	AA <sub>H</sub>	X554 <sub>H</sub>	55 <sub>H</sub>	XAAA <sub>H</sub>	80 <sub>H</sub>	XAAA <sub>H</sub>	AA <sub>H</sub>	X554 <sub>H</sub>	55 <sub>H</sub>	XAAA <sub>H</sub>	$10_{\rm H}$

• RA : Read address

• PA : Write (program) address

• RD : Read data

• PD : Write (program) data

• U : Upper 4 bits same as RA, PA, and SA

• F<sub>X</sub> : FF/FE

• X : Arbitrary address

\*: Both of the two types of read/reset command can reset the flash memory to read mode.

#### Notes:

- Addresses in the table are the values in the CPU memory map. All addresses and data are hexadecimal values. However, "X" is an arbitrary value.
- Address "U" in the table is not arbitrary, whose four bits (bits 15 to 12) must have the same value as RA and PA.

Example: If RA = C48EH, U = C; If PA = 1024H, U=1

#### Notes on Issuing Commands

Pay attention to the following points when issuing commands in the command sequence table:

The upper address U bits (bits 15 to 12) used when commands are issued must have the same value as RA and PA, from the first command on.

If the above measures are not followed, commands are not recognized normally. Execute a reset to initialize the command sequencer in the flash memory.

## 25.5 Checking the Automatic Algorithm Execution Status

#### As the flash memory uses the automatic algorithm for a process flow for programming/ erasing, you can check its internal operating status with hardware sequence flags.

#### ■ Hardware Sequence Flag

• Overview of hardware sequence flag

The hardware sequence flag consists of the following 5-bit outputs:

- Data polling flag (DQ7)
- Toggle bit flag (DQ6)
- Execution time-out flag (DQ5)
- Toggle bit 2 flag (DQ2)

The hardware sequence flags tell whether the write (program) or chip-erase command has been terminated and whether an erase code write can be performed.

You can reference hardware sequence flags by read access to the address of each relevant sector in flash memory after setting a command sequence. Note, however, that hardware sequence flags are output only for the bank on a command-issued side.

Table 25.5-1 shows the bit allocation of the hardware sequence flags.

#### Table 25.5-1 Bit Allocation of Hardware Sequence Flags

Bit No.	7	6	5	4	3	2	1	0
Hardware sequence flag	DQ7	DQ6	DQ5	-	-	DQ2	-	-

- To know whether the automatic write or chip-erase command is being executed or has been terminated, check the hardware sequence flags or the flash memory program/erase status bit in the flash memory status register (FSR:RDY). After programming/erasing is terminated, flash memory returns to the read/ reset state.
- When creating a write/erase program, read data after checking the termination of automatic writing/ erasing with the DQ7, DQ6, DQ5, and DQ2 flags.

#### • Explanation of hardware sequence flag

Table 25.5-2 lists the functions of the hardware sequence flag.

#### Table 25.5-2 List of Hardware Sequence Flag Functions

	State	DQ7	DQ6	DQ5	DQ2
State transition	Programming $\rightarrow$ Programming completed (when write address has been specified)	$\overline{\text{DQ7}} \rightarrow \\ \text{DATA: 7}$	Toggle → DATA: 6	$\begin{array}{c} 0 \rightarrow \\ \text{DATA: 5} \end{array}$	$1 \rightarrow$ DATA:2
operation	Chip erasing $\rightarrow$ Erasing completed	$0 \rightarrow 1$	$\begin{array}{c} \text{Toggle} \rightarrow \\ \text{Stop} \end{array}$	$0 \rightarrow 1$	Toggle → Stop
Abnormal	Programming	DQ7	Toggle	1	1
operation	Chip erasing	0	Toggle	1	*

\*: When the DQ5 flag is 1 (execution time-out), the DQ2 flag toggles during continuous reading from the programming/erasing sector but does not toggle during reading from other sectors.
## 25.5.1 Data Polling Flag (DQ7)

# The data polling flag (DQ7) is a hardware sequence flag used to indicate that the automatic algorithm is being executing or has been completed using the data polling function.

### ■ Data Polling Flag (DQ7)

Table 25.5-3 and Table 25.5-4 show the state transition of the data polling flag.

### Table 25.5-3 State Transition of Data Polling Flag (During Normal Operation)

$Operating state \qquad Programming \rightarrow Programming completed$		Chip erasing $\rightarrow$ Erasing completed		
DQ7	$\overline{\text{DQ7}} \rightarrow \text{DATA: 7}$	01		

### Table 25.5-4 State Transition of Data Polling Flag (During Abnormal Operation)

Operating state	Programming	Chip erasing
DQ7	DQ7	0

### • At programming

When read access takes place during execution of the automatic write algorithm, the flash memory outputs the inverted value of bit 7 in the last data written to DQ7.

If read access takes place on completion of the automatic write algorithm, the flash memory outputs bit 7 of the value read from the read-accessed address to DQ7.

### • At chip erasing

When read access is made to the sector currently being erased during execution of the chip erase algorithm, bit 7 of flash memory outputs "0". Bit 7 of flash memory outputs "1" upon completion of chip erasing.

### Note:

Once the automatic algorithm has been started, read access to the specified address is ignored. Data reading is allowed after the data polling flag (DQ7) is set to "1". Data reading after the end of the automatic algorithm should be performed following read access made to confirm the completion of data polling.

# 25.5.2 Toggle Bit Flag (DQ6)

# The toggle bit flag (DQ6) is a hardware sequence flag used to indicate that the automatic algorithm is being executed or has been completed using the toggle bit function.

### ■ Toggle Bit Flag (DQ6)

Table 25.5-5 and Table 25.5-6 show the state transition of the toggle bit flag.

### Table 25.5-5 State Transition of Toggle Bit Flag (During Normal Operation)

$Operating state \qquad Programming \rightarrow Programming completed$		Chip erasing $\rightarrow$ Erasing completed		
DQ6	Toggle $\rightarrow$ DATA: 6	$Toggle \rightarrow Stop$		

### Table 25.5-6 State Transition of Toggle Bit Flag (During Abnormal Operation)

Operating state	Programming	Chip erasing
DQ6	Toggle	Toggle

• At programming and chip erasing

- When read access is made continuously during execution of the automatic write algorithm or chip-erase algorithm, the flash memory toggles the output between "1" and "0" at each read access.
- When read access is made continuously after the automatic write algorithm or chip-erase algorithm is terminated, the flash memory outputs bit 6 (DATA:6) of the value read from the read address at each read access.

### 25.5.3 Execution Time-out Flag (DQ5)

# The execution time-out flag (DQ5) is a hardware sequence flag indicating that the automatic algorithm has been executed beyond the specified time (required for programming/erasing) internal to the flash memory.

### ■ Execution Time-out Flag (DQ5)

Table 25.5-7 and Table 25.5-8 show the state transition of the execution time-out flag.

### Table 25.5-7 State Transition of Execution Time-out Flag (During Normal Operation)

$Operating \ state \qquad Programming \rightarrow Programming \ completed$		$Chip \ erasing \rightarrow Erasing \ completed$	
DQ5	$0 \rightarrow \text{DATA: 5}$	$0 \rightarrow 1$	

### Table 25.5-8 State Transition of Execution Time-out Flag (During Abnormal Operation)

Operating state	Programming	Chip erasing
DQ5	1	1

### • At programming and chip erasing

When read access is made with the write or chip-erase automatic algorithm invoked, the flag outputs "0" when the algorithm execution time is within the specified time (required for programming/erasing) or "1" when it exceeds that time.

The execution time-out flag (DQ5) can be used to check whether programming/erasing has succeeded or failed regardless of whether the automatic algorithm has been running or terminated. When the execution time-out flag (DQ5) outputs "1", it indicates that programming has failed if the automatic algorithm is still running for the data polling or toggle bit function.

If an attempt is made to write "1" to a flash memory address holding "0", for example, the flash memory is locked, preventing the automatic algorithm from being terminated and valid data from being output from the data polling flag (DQ7). As the toggle bit flag (DQ6) does not stop toggling, the time limit is exceeded and the execution time-out flag (DQ5) outputs "1". The state in which the execution time-out flag (DQ5) outputs "1" means that the flash memory has not been used correctly; it does not mean that the flash memory is defective. When this state occurs, execute the reset command.

# 25.5.4 Toggle Bit 2 Flag (DQ2)

# The toggle bit 2 flag (DQ2) is a hardware sequence flag used to indicate that chiperasing is executed using the toggle bit function.

### ■ Toggle Bit 2 Flag (DQ2)

Table 25.5-9 and Table 25.5-10 show the state transition of the toggle bit 2 flag.

### Table 25.5-9 State Transition of Toggle Bit 2 Flag (During Normal Operation)

Operating state $Programming \rightarrow Programming completed$		Chip erasing $\rightarrow$ Erasing completed	
DQ2	$1 \rightarrow \text{DATA: } 2$	$Toggle \rightarrow Stop$	

### Table 25.5-10 State Transition of Toggle Bit 2 Flag (During Abnormal Operation)

Operating state	Programming	Chip erasing
DQ2	1	*

\*: When the DQ5 flag is 1 (execution time-out), the DQ2 flag toggles during continuous reading from the programming/erasing sector but does not toggle during reading from other sectors.

### • At chip erasing

- When read access is made continuously during execution of the chip-erase algorithm, the flash memory toggles the output between "1" and "0" at each read access.
- When read access is made continuously after the chip-erase algorithm is terminated, the flash memory outputs bit 2 (DATA:2) of the value read from the read address at each read access.

# 25.6 Details of Programming/Erasing Flash Memory

This section describes the individual procedures for flash memory reading/resetting, programming, and chip-erasing by entering their respective commands to invoke the automatic algorithm.

### Details of Programming/Erasing Flash Memory

The automatic algorithm can be invoked by writing the read/reset, program, and chip-erase command sequence to flash memory from the CPU. Writing command sequence to flash memory from the CPU must always be performed continuously. The termination of the automatic algorithm can be checked by the data polling function. After the automatic algorithm terminates normally, the flash memory returns to the read/ reset state.

The individual operations are explained in the following order:

- Enter read/reset state.
- Program data.
- Erase all data (chip-erase).

### 25.6.1 Placing Flash Memory in the Read/Reset State

# This section explains the procedure for entering the read/reset command to place flash memory in the read/reset state.

### Placing Flash Memory in the Read/Reset State

- To place flash memory in the read/reset state, send the read/reset command in the command sequence table continuously from the CPU to flash memory.
- The read/reset command is available in two different command sequences: one involves a single bus operation and the other involves four bus operations, which are essentially the same.
- Since the read/reset state is the initial state of flash memory, the flash memory always enters this state after the power is turned on and at the normal termination of a command. The read/reset state is also described as the wait state for command input.
- In the read/reset state, read access to flash memory enables data to be read. As is the case with masked ROM, program access from the CPU can be made.
- Read access to flash memory does not require the read/reset command. If a command is not terminated normally, use the read/reset command to initialize the automatic algorithm.

### 25.6.2 Programming Data into Flash Memory

# This section explains the procedure for entering the write (program) command to program data into flash memory.

### Programming Data into Flash Memory

- To start the automatic algorithm for programming data into flash memory, send the program command in the command sequence table continuously from the CPU to flash memory.
- Upon completion of data programming to a target address in the fourth cycle, the automatic algorithm starts automatic programming.
- How to specify addresses
  - Programming (writing) can be performed even in any order of addresses or across a sector boundary. Data written by a single program command is only one byte.
- Notes on programming data
  - Bit data cannot be returned from "0" to "1" by programming. When bit data "1" is programmed to bit data "0", the data polling algorithm (DQ7) or toggle operation (DQ6) is not terminated, the flash memory element is determined to be defective, and the execution time-out flag (DQ5) detects an error to indicate that the specified programming time has been exceeded.

When data is read in the read/reset state, the bit data remains "0". To return the bit data from "0" to "1", erase flash memory.

- All commands are ignored during automatic programming.
- If a hardware reset occurs during programming, the data being programmed to the current address is not guaranteed. Retry from the chip-erase command.

### Flash Memory Programming Procedure

- Figure 25.6-1 gives an example of the procedure for programming data into flash memory. The hardware sequence flags can be used to check the operating state of the automatic algorithm in flash memory. The data polling flag (DQ7) is used for checking the completion of programming into flash memory in this example.
- Flag check data should be read from the address where data was last written.
- Because the data polling flag (DQ7) and execution time-out flag (DQ5) are updated at the same time, the data polling flag (DQ7) must be checked even when the execution time-out flag (DQ5) is "1".
- Similarly, the toggle bit flag (DQ6) must be checked as it stops toggling at the same time as when the execution time-out flag (DQ5) changes to "1".



Figure 25.6-1 Sample Procedure for Programming into Flash Memory

# 25.6.3 Erasing All Data from Flash Memory (Chip Erase)

# This section describes the procedure for issuing the chip erase command to erase all data from flash memory.

### Erasing Data from Flash Memory (Chip Erase)

- To erase all data from flash memory, send the chip erase command in the command sequence table continuously from the CPU to flash memory.
- The chip erase command is executed in six bus operations. Chip erasing is started upon completion of the sixth programming cycle.
- Before chip erasing, the user need not perform programming into flash memory. During execution of the automatic erase algorithm, flash memory automatically programs "0" before erasing all cells automatically.

### Notes on Chip Erasing

If a hardware reset occurs during erasure, the data being erased from flash memory is not guaranteed.

### 25.7 Features of Flash Security

# The flash security controller function prevents the contents of flash memory from being read through external pins.

### Features of Flash Security

Writing protection code " $01_{\text{H}}$ " to a flash memory address ( $8000_{\text{H}}$ ) restricts access to flash memory, barring read/write access to flash memory from any external pin. Once flash memory has been protected, the function cannot be unlocked until the chip erase command is executed.

Note that only addresses  $5554_{\text{H}}$  and  $2AAA_{\text{H}}$  can be read as exceptions.

It is advisable to code the protection code at the end of flash programming. This is to avoid unnecessary protection during programming.

Once flash memory has been protected, the chip erase operation is required before it can be reprogrammed.

For details, ask your local representative of Fujitsu.

# CHAPTER 26 EXAMPLE OF SERIAL PROGRAMMING CONNECTION

This chapter describes the example of a serial programming connection.

- 26.1 Basic Configuration of the Flash Memory Products Serial Programming Connection
- 26.2 Example of Serial Programming Connection
- 26.3 Example of Minimum Connection to Flash Microcomputer Programmer

## 26.1 Basic Configuration of the Flash Memory Products Serial Programming Connection

# The MB95F136MS, NS/MW, NW supports flash ROM serial onboard programming (Fujitsu standard).

This section describes the specifications.

### ■ Basic Configuration of the Flash Memory Products Serial Programming Connection

The AF220/AF210/AF120/AF110 flash microcomputer programmer manufactured by YokogawaDigital Computer Co., Ltd. is used for Fujitsu standard serial onboard programming.

Figure 26.1-1 shows the basic configuration of MB95F136MS, NS/MW, NW serial programming connection.

### Figure 26.1-1 Basic Configuration of the Flash Memory Products Serial Programming Connection



Note:

For the function and operation method of the AF220/AF210/AF120/AF110 flash microcomputer programmer and the general-purpose common cable (AZ210) and connector, contact Yokogawa Digital Computer Co., Ltd.

Pin	Function	Description
MOD, P13	Mode pin	Setting MOD=High and P13=Low sets serial write mode.
X0, X1	Oscillation pins	The CPU's internal operating clock during serial write mode is the oscillator frequency divided by two. Note that a 1MHz or higher oscillator frequency must be input when performing serial writing.
RST	Reset pin	-
P10/UI0	Serial data input pin	Setting P10/UI0=Low specifies that serial write mode uses clock synchronous communications. As this low input is handled by the TTXD pin of the flash microcomputer programmer, you do not need to provide a pull-down for the P10/UI0 pin.
P11/UO0	Serial data output pin	-
P12/UCK0	Serial clock input pin	Setting P12/UCK0=High sets serial write mode. As this high input is handled by the TCK pin of the flash microcomputer programmer, you do not need to provide a pull-up for the P12/UCK0 pin.
V <sub>CC</sub>	Power supply voltage supply pin	On the MB95F136MS, NS/MW, NW, the write voltage ( $Vcc = 4.5V$ to 5.5V) is supplied from the user system.
V <sub>SS</sub>	GND pin	Common to the GND of the flash microcomputer programmer.

Table 26.1-1 Pins Used for Fujitsu Standard Serial Onboard Programming

As the UI0, UO0, and UCK0 pins are also used by the user system, you need to provide a control circuit as shown in Figure 26.1-2 if you want to disconnect from the user circuit during serial writing.

(The /TICS signal of the flash microcomputer programmer can be used to disconnect from the user circuit during serial writing. See the connection example in Figure 26.1-2 for details.)





### • Oscillation Clock Frequency and Serial Clock Input Frequency

The permitted frequency for the input serial clock on the MB95F136MS, NS/MW, NW is calculated from the following formula. Accordingly, adjust the settings on the flash microcomputer programmer so that the serial clock input frequency matches the oscillation clock frequency being used.

Permitted frequency for the input serial clock =  $0.125 \times \text{Oscillation clock frequency}$ 

### Example:

Oscillation clock frequency	Maximum serial clock frequency that can be input to the microcomputer	Maximum serial clock frequency that can be set on the AF220, AF210, AF120, and AF110	Maximum serial clock frequency that can be set on the AF200
at 4MHz	500kHz	500kHz	500kHz
at 8MHz	1MHz	850kHz	500kHz
at 10MHz	1.25MHz	1.25MHz	500kHz

### Table 26.1-2 System Configuration of the Flash Microcomputer Program (Yokogawa Digital Computer Co., Ltd.)

Туре		Function		
	AF220/AC4P	Model with built-in Ethernet interface	/100V to 220V power adapter	
Main	AF210/AC4P	Standard model	/100V to 220V power adapter	
unit	AF120/AC4P	Single-key model with built-in Ethernet interface	/100V to 220V power adapter	
	AF110/AC4P	Single-key model	/100V to 220V power adapter	
AZ221	Writer-dedicated RS232C cable for PC/AT			
AZ210		Standard target probe (a) Length: 1 m		
FF201		Fujitsu control module for flash microcomputer		
AZ290		Remote controller		
/P2 2Mbytes PC Card (Option) Flash memory capacity: up to 128 Kbytes		y: up to 128 Kbytes		
/P4	/P4 4Mbytes PC Card (Option) Flash memory capacity: up to 512 Kbytes		y: up to 512 Kbytes	

Contact address: Yokogawa Digital Computer Co., Ltd. Tell: +81-042-333-6222

Note:

Although the AF200 flash microcomputer programmer is an old model, this can be handled using the FF201 control module. The connection examples shown in the next chapter can also be used as example connections for serial writing.

# 26.2 Example of Serial Programming Connection

Inputting MOD="H" from TAUX3 on the AF220, AF210, AF120, or AF110 to the mode pin, which is set to MOD="L" by the user system, sets the mode to serial write mode (serial write mode: MOD="H", P12="H", P13="L").

### Example of Serial Programming Connection

Figure 26.2-1 shows an example connection for serial writing.

The TTXD pin on the flash microcomputer programmer is connected to P10/UI0 and outputs low until data transfer starts. Setting P10/UI0=Low in this way specifies that serial write mode uses clock synchronous communications.

Note that a user power supply is required for serial writing.





The circuit [1] shown in Figure 26.2-1 is required if you want to disconnect the UCK0 and  $\overline{\text{RST}}$  pins from the user circuit during serial writing (The /TICS signal of the flash microcomputer programmer outputs low during serial writing and this disconnects the user circuit).

If it is not necessary to disconnect from the user circuit, the connection to /TICS and circuit [1] are not required. See the connection example in Figure 26.3-1.

The UI0 and UO0 pins are also used by the user system and the control circuit shown below like that used for the UCK0 pin is required if you want to disconnect from the user circuit during serial writing (The /TICS signal of the flash microcomputer programmer can be used to disconnect from the user circuit during serial writing. See the connection example in Figure 26.1-2 for details)



Only connect to the AF220, AF210, AF120, or AF110 while the user power supply is turned off.

Note:

The pull-up and pull-down resistances in the above example connection are examples only and may be adjusted to suit your system. If variation in the input level to the MOD pin is possible due to noise or other factors, it is also recommended that you use a capacitor or other method to minimize noise.

# 26.3 Example of Minimum Connection to Flash Microcomputer Programmer

The connection between MOD and the flash microcomputer programmer is not required if the pins are set as shown in Figure 26.3-1 during serial writing (serial write mode: MOD="H", P12="H", P13="L").

### Example of Minimum Connection to Flash Microcomputer Programmer

Figure 26.3-1 shows an example of the minimum possible connection to the flash microcomputer programmer.

The TTXD pin on the flash microcomputer programmer is connected to P10/UI0 and outputs low until data transfer starts. Setting P10/UI0=Low in this way specifies that serial write mode uses clock synchronous communications.

Note that a user power supply is required for serial writing.

### Figure 26.3-1 Example of Minimum Connection to MB95F136MS,NS/MW,NW Flash Microcomputer Programmer



As the UI0, UO0, and UCK0 pins are also used by the user system, you need to provide a control circuit as shown below if you want to disconnect from the user circuit during serial writing (The /TICS signal of the flash microcomputer programmer can be used to disconnect from the user circuit during serial writing. See the connection example in Figure 26.2-1 for details).



Only connect to the AF220, AF210, AF120, or AF110 while the user power supply is turned off.

Note:

The pull-up and pull-down resistances in the above example connection are examples only and may be adjusted to suit your system. If variation in the input level to the MOD pin is possible due to noise or other factors, it is also recommended that you use a capacitor or other method to minimize noise.

# APPENDIX

This appendix explains I/O map, interrupt list, memory map, pin status, instruction overview, mask option and writing to Flash microcomputer using parallel writer.

APPENDIX AI/O MapAPPENDIX BTable of Interrupt CausesAPPENDIX CMemory MapAPPENDIX DPin Status of MB95130/M seriesAPPENDIX EInstruction OverviewAPPENDIX FMask OptionAPPENDIX GWriting to Flash Microcontroller Using Parallel Writer

# APPENDIX A I/O Map

### This section explains I/O map that is used on MB95130/M series.

### ■ I/O Map

### Table A-1 MB95130/M Series (1 / 4)

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>		(Do Not Use)		
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	PLLC	PLL control register	R/W	00000000 <sub>B</sub>
0007 <sub>H</sub>	SYCC	System clock control register	R/W	1010x011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	00000000 <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset cause register	R	xxxxxxxB
000A <sub>H</sub>	TBTC	Timebase timer control register	R/W	$0000000_{\rm B}$
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	$00000000_{\rm B}$
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	$00000000_{\rm B}$
000D <sub>H</sub>				•
to 0027 <sub>H</sub>		(Do Not Use)		
0028 <sub>H</sub>	PDRF	Port F data register	R/W	00000000 <sub>B</sub>
0029 <sub>H</sub>	DDRF	Port F direction register	R/W	00000000 <sub>B</sub>
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	PUL0	Port 0 pull-up register	R/W	00000000 <sub>B</sub>
002D <sub>H</sub>	PUL1	Port 1 pull-up register	R/W	00000000 <sub>B</sub>
002E <sub>H</sub>				
to		(Do Not Use)		
0034 <sub>H</sub>			D (11)	0000000
0035 <sub>H</sub>	PULG	Port G pull-up register	R/W	00000000 <sub>B</sub>
0036 <sub>H</sub>	TOICRI	8/16-bit composite timer 01 control status register 1 ch.0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	TOOCRI	8/16-bit composite timer 00 control status register 1 ch.0	R/W	00000000B
0038 <sub>H</sub> 0039 <sub>H</sub>		(Do Not Use)		
003A11	PC01	8/16-bit PPG1 control register ch 0	R/W	0000000
003Bu	PC00	8/16-bit PPG0 control register ch.0	R/W	0000000р

### Table A-1 MB95130/M Series (2 / 4)

Address	Register abbreviation	Register     Register name       abbreviation     Register name					
003C <sub>H</sub>							
to		(Do Not Use)					
0041 <sub>H</sub>				0000000			
0042 <sub>H</sub>	PCNTH0	16-bit PPG status control register upper ch.0	R/W	00000000 <sub>B</sub>			
0043 <sub>H</sub>	PCNTL0	16-bit PPG status control register lower ch.0	R/W	00000000 <sub>B</sub>			
0044 <sub>H</sub>		(Do Not Use)					
0047 <sub>н</sub>		(Do Not Use)					
0048 <sub>H</sub>	EIC00	External interrupt circuit control register ch.0/1	R/W	00000000 <sub>B</sub>			
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch.2/3	R/W	00000000 <sub>B</sub>			
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch.4/5	R/W	00000000 <sub>B</sub>			
004B <sub>H</sub>	EIC30	R/W	00000000 <sub>B</sub>				
004C <sub>H</sub>							
to		(Do Not Use))					
$004F_{H}$							
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>			
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>			
0052 <sub>H</sub>	SSR LIN-UART serial status register		R/W	00001000			
0053 <sub>H</sub>	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000 <sub>B</sub>			
0054 <sub>H</sub>	ESCR LIN-UART extended status control register		R/W	00000100 <sub>B</sub>			
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>			
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1 ch.0	R/W	00000000 <sub>B</sub>			
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2 ch.0	R/W	00100000 <sub>B</sub>			
0058 <sub>H</sub>	SSR0	UART/SIO serial status and data register ch.0	R/W	00000001 <sub>B</sub>			
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register ch.0	R/W	00000000 <sub>B</sub>			
005A <sub>H</sub>	RDR0	UART/SIO serial input data register ch.0	R	00000000 <sub>B</sub>			
005B <sub>H</sub>							
to		(Do Not Use)					
006B <sub>H</sub>	1001		DAV	0000000			
000C <sub>H</sub>	ADCI	A/D control register 1	R/W	0000000 <sub>B</sub>			
006D <sub>H</sub>	ADC2	A/D control register 2	K/W	00000000B			
000EH	ADDH	A/D data register upper	R/W	00000000B			
000F <sub>H</sub>	ADDL	A/D data register lower	R/W	0000000B			
0070 <sub>H</sub>	WCSR	Watch counter control register	R/W	0000000 <sub>B</sub>			
00/1 <sub>H</sub>	FCD	(Do Not Use)		000-0000			
0072 <sub>H</sub>	FSR	Flash memory status register	K/W	00000000B			
0073 <sub>H</sub>	SWRE0	Flash memory sector write control register 0	K/W	00000000B			
0074 <sub>H</sub>	SWREI	Flash memory sector write control register 1	K/W	00000000B			
00/5 <sub>H</sub>		(Do Not Use)		0000000			
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000B			
00// <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>			

### Table A-1 MB95130/M Series (3 / 4)

Address	Register abbreviation	Register Register name				
0078 <sub>H</sub>		Register bank pointer (RP), Mirror of direct bank register (DP)				
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>		
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>		
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>		
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>		
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>		
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>		
$007F_{H}$		(Do Not Use)	4			
0F80 <sub>H</sub>	WRARH0	Wild register address setup register upper ch.0	R/W	$0000000_{\rm B}$		
0F81 <sub>H</sub>	WRARL0	Wild register address setup register lower ch.0	R/W	$00000000_{\rm B}$		
0F82 <sub>H</sub>	WRDR0	Wild register data setup register ch.0	R/W	$00000000_{\rm B}$		
0F83 <sub>H</sub>	WRARH1	Wild register address setup register upper ch.1	R/W	$00000000_{\rm B}$		
0F84 <sub>H</sub>	WRARL1	Wild register address setup register lower ch.1	R/W	$00000000_{\rm B}$		
0F85 <sub>H</sub>	WRDR1	Wild register data setup register ch.1	R/W	00000000 <sub>B</sub>		
0F86 <sub>H</sub>	WRARH2	Wild register address setup register upper ch.2	R/W	00000000 <sub>B</sub>		
0F87 <sub>H</sub>	WRARL2	Wild register address setup register lower ch.2	R/W	00000000 <sub>B</sub>		
0F88 <sub>H</sub>	WRDR2	Wild register data setup register ch.2	R/W	00000000 <sub>B</sub>		
0F89 <sub>H</sub>			.1			
to		(Do Not Use)				
0F91 <sub>H</sub>			<u>,                                    </u>			
0F92 <sub>H</sub>	T01CR0	8/16-bit composite timer 01 control status register 0 ch.0	R/W	00000000 <sub>B</sub>		
0F93 <sub>H</sub>	T00CR0	8/16-bit composite timer 00 control status register 0 ch.0	R/W	00000000 <sub>B</sub>		
0F94 <sub>H</sub>	T01DR	8/16-bit composite timer 01 data register ch.0	R/W	00000000 <sub>B</sub>		
0F95 <sub>H</sub>	TOODR	8/16-bit composite timer 00 data register ch.0	R/W	00000000 <sub>B</sub>		
0F96 <sub>H</sub>	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch.0	R/W	00000000 <sub>B</sub>		
0F97 <sub>H</sub>						
to OFOB		(Do Not Use)				
0F9Cu	PPS01	8/16 bit PPG01 cycle setting buffer register ch 0	P/W	11111111		
0F9D <sub>11</sub>	PPS00	8/16 bit PPG00 cycle setting buffer register ch.0		11111111 <sub>b</sub>		
0F9Eu	PDS01	8/16-bit PPG01 duty setting buffer register ch 0	R/W	11111111 <sub>D</sub>		
0F9Eu	PDS00	8/16-bit PPG00 duty setting buffer register ch.0	R/W	11111111 <sub>D</sub>		
OFA0 <sub>11</sub>	10500	8/10-bit 11 000 duty setting burter register ento	K/ W	IIIIIIB		
to		(Do Not Use)				
0FA3 <sub>H</sub>						
0FA4 <sub>H</sub>	PPGS	8/16-bit PPG startup register	R/W	00000000 <sub>B</sub>		
0FA5 <sub>H</sub>	REVC	8/16-bit PPG output reverse register	R/W	00000000 <sub>B</sub>		
0FA6 <sub>H</sub>			1			
to		(Do Not Use)				
0FA9 <sub>H</sub>						
0FAA <sub>H</sub>	PDCRH0	16-bit PPG down counter register upper ch.0	R	$00000000_{\rm B}$		

### Table A-1 MB95130/M Series (4 / 4)

Address	Register abbreviation	Register name	R/W	Initial value
0FAB <sub>H</sub>	PDCRL0	16-bit PPG down counter register lower ch.0	R	00000000 <sub>B</sub>
0FAC <sub>H</sub>	PCSRH0	16-bit PPG cycle setting buffer register upper ch.0	R/W	11111111 <sub>B</sub>
0FAD <sub>H</sub>	PCSRL0	16-bit PPG cycle setting buffer register lower ch.0	R/W	11111111 <sub>B</sub>
0FAE <sub>H</sub>	PDUTH0	16-bit PPG duty setting buffer register upper ch.0	R/W	11111111 <sub>B</sub>
0FAF <sub>H</sub>	PDUTL0	16-bit PPG duty setting buffer register lower ch.0	R/W	11111111 <sub>B</sub>
0FB0 <sub>H</sub> to 0FBB <sub>H</sub>		(Do Not Use)		
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0 UART/SIO prescaler select register ch.0			00000000 <sub>B</sub>
0FBF <sub>H</sub>	BRSR0	R/W	00000000 <sub>B</sub>	
0FC0 <sub>H</sub> to 0FC2 <sub>H</sub>		(Do Not Use)		
0FC3 <sub>H</sub>	AIDRL	A/D input disable register lower	R/W	00000000 <sub>B</sub>
0FC4 <sub>H</sub> to 0FE2 <sub>H</sub>		(Do Not Use)		
0FE3 <sub>H</sub>	WCDR	Watch counter data register	R/W	00111111 <sub>B</sub>
0FE4 <sub>H</sub> to 0FE6 <sub>H</sub>		(Do Not Use)		
0FE7 <sub>H</sub>	ILSR2	Input level selection register 2	R/W	0000000 <sub>B</sub>
0FE8 <sub>H</sub> to 0FED <sub>H</sub>		(Do Not Use)		
0FEE <sub>H</sub>	ILSR	Input level selection register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub>	WICR	Interrupt pin control register	R/W	01000000 <sub>B</sub>
0FF0 <sub>H</sub> to 0FFF <sub>H</sub>		(Do Not Use)		

# **APPENDIX B** Table of Interrupt Causes

### This section describes the table of interrupt causes used in MB95130/M series.

### ■ Table of Interrupt Causes

Refer to "CHAPTER 5 CPU" for interrupt operation.

### Table B-1 MB95130/M Series

Interrupt causes	Interrupt request	Add of vecto	ress or table	Bit name of interrupt level	The same level priority (Concurrence)	
	number	Upper	Lower	setting register		
External interrupt ch.0	IPO0	FFFA	FFFR	L 00 [1:0]	High	
External interrupt ch.4		IIIAH	IIIDH	L00 [1.0]	<b></b>	
External interrupt ch.1	IRO1	FFF8	FFF9.	I 01 [1:0]		
External interrupt ch.5	IKQI	III 0H	III) <sub>H</sub>	L01 [1.0]		
External interrupt ch.2	IRO2	FFF611	FFF7.	L 02 [1:0]		
External interrupt ch.6	IKQ2	III °H	ιι, <sub>H</sub>	L02 [1.0]		
External interrupt ch.3	IRO3	FFF411	FFF51	1.03 [1:0]		
External interrupt ch.7	IKQ5	H	III o H	105 [1.0]		
UART/SIO ch.0	IRQ4	$FFF2_{H}$	FFF3 <sub>H</sub>	L04 [1:0]		
8/16-bit composite timer ch.0 (lower)	IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]		
8/16-bit composite timer ch.0 (upper)	IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1:0]		
LIN-UART (reception)	IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1:0]		
LIN-UART (transmission)	IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1:0]		
(Not used)	IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]		
(Not used)	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1:0]		
(Not used)	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1:0]		
8/16-bit PPG ch.0 (upper)	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]		
8/16-bit PPG ch.0 (lower)	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]		
(Not used)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1:0]		
16-bit PPG ch.0	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1:0]		
(Not used)	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]		
(Not used)	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]		
10-bit A/D	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1:0]		
Timebase timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]		
Watch prescaler/counter	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]		
(Not used)	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]		
(Not used)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1:0]	★	
FLASH	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1:0]	Low	

# APPENDIX C Memory Map

### This section shows the memory map of MB95130/M series.

### Memory Map

Figure C-1 Memory Map								
	MB95FV100D-101 MB95FV100D-103		MB95136M	MB9 MB9 MB95 MB95 MB95	5F133MS/F133NS 5F134MS/F134NS 5F136MS/F136NS 5F133MW/F133NW 5F134MW/F134NW 5F136MW/F136NW			
0000 <sub>H</sub>	I/O	0000 <sub>H</sub>	I/O	0000 <sub>H</sub>	I/O			
0080 <sub>H</sub> 0100 <sub>H</sub>	RAM 3.75K bytes	0080 <sub>H</sub> 0100⊔	RAM 1K bytes	0080 <sub>H</sub> 0100⊔	RAM			
0200 <sub>H</sub>	Registers	0200 <sub>H</sub>	Registers	0200 <sub>H</sub>	Registers			
		0480 <sub>H</sub>	Access prohibited	Address #1	Access prohibited			
0F80 <sub>H</sub>	Extended I/O	0F80 <sub>H</sub>	Extended I/O	0F80 <sub>H</sub>	Extended I/O			
1000 <sub>H</sub>		1000 <sub>H</sub>		1000 <sub>H</sub>				
			Access prohibited		Access prohibited			
	Flash 60K bytes	8000 <sub>H</sub>		Address #2				
			ROM 32K bytes		Flash memory			
FFFF <sub>H</sub>		FFFF <sub>H</sub>		FFFF <sub>H</sub>				
Flash : ROM :	Flash memory Mask ROM	FFFFH FFFH FFFH FFFH FFFH FFFH FFFH FF						

	Flash memory	RAM	Address #1	Address #2	
MB95F133MS/F133NS	8 Khytas	256 bytes	0180	E000	
MB95F133MW/F133NW	8 KUyles	250 bytes	0180 <sub>H</sub>	E000H	
MB95F134MS/F134NS	16 Vbutas	512 hyter	0380	C000	
MB95F134MW/F134NW	10 KDytes	512 bytes	0280 <sub>H</sub>	$C000_{\rm H}$	
MB95F136MS/F136NS	20 Khutaa	1 Khutaa	0.480	8000	
MB95F136MW/F136NW	52 KDytes	1 Köytes	0480 <sub>H</sub>	8000H	

# APPENDIX D Pin Status of MB95130/M series

### The state of the terminal of the MB95130/M series in each mode is shown in Table D-1.

### ■ Pin Status in Each Mode

### Table D-1 Pin Status in Each Mode (1 / 2)

Din namo	Normal	Sloop mode	Stop mode		Watch mode		While
Finname	operation	Sleep mode	SPL=0	SPL=1	SPL=0	SPL=1	resetting
X0	Oscillation circuit input	Oscillation circuit input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Oscillation circuit input
X1	Oscillation circuit output	Oscillation circuit input	"H"	"H"	"H"	"H"	Oscillation circuit output
MOD	Mode input	Mode input	Mode input	Mode input	Mode input	Mode input	Mode input
RST	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input
P00/INT00/ AN00/ PPG00							
P01/INT01/ AN01/ PPG01				Hi-Z (However, the		Hi-Z (However, the	
P02/INT02/ AN02/SCK				setting of the pull-up is		setting of the pull-up is	
P03/INT03/ AN03/SOT	I/O port/ peripheral	I/O port/ peripheral	I/O port/ peripheral	Input interception	I/O port/ peripheral	Input interception	Hi-Z
P04/INT04/ AN04/SIN	function I/O/ Analog input	function I/O/ Analog input	function I/O/ Analog input	(However, an external	function I/O/ Analog input	(However, an external	Input disable <sup>*2</sup>
P05/INT05/ AN05/ TO00				the external interrupt is		the external interrupt is	
P06/INT06/ AN06/ TO01				enable.)		enable.)	
P07/INT07/ AN07							

Din namo	Rin name Normal		Stop	Stop mode		Watch mode		
Finname	operation	Sleep mode	SPL=0 SPL=1 SPL=0		SPL=0	SPL=1	resetting	
P10/UI0								
P11/UO0								
P12/UCK0/ EC0	I/O port/	I/O port/	I/O port/	H1-Z (However, the setting of the	I/O port/	H1-Z (However, the setting of the	Hi-Z Input enable <sup>*1</sup>	
P13/TRG0/ ADTG	peripheral function I/O	peripheral function I/O	peripheral function I/O	pull-up is effective.)	peripheral function I/O	pull-up is effective.)	(However, it doesn't	
P14/PPG0	-			Input interception		Input interception	function.)	
P15								
P16								
PF0							Hi-Z	
PF1	I/O port	I/O port	I/O port	Hi-Z Input interception	I/O port	Hi-Z Input interception	Input enable <sup>*1</sup> (However, it doesn't function.)	
PG0							Hi-Z	
PG1	I/O port	I/O port	I/O port	Hi-Z Input	I/O port	Hi-Z Input	Input enable <sup>*1</sup>	
PG2	I/O port	D port I/O port I/		interception		interception	(However, it doesn't function. )	

Table D-1 Pin Status in Each Mode (2 / 2)

SPL: Pin status specification bit of standby control register (STBC: SPL)

Hi-Z: High impedance

\*1: "Input enable" means the input function is possible. Therefore, it is necessary to process the pull-up and the pull-down or to prevent leakage being generated by the input from the outside. It is the same status as other ports when using it as an output port.

\*2: "Input disable" means direct input gate operation from the terminal is disable status.

# **APPENDIX E** Instruction Overview

### This section explains the instructions used in $F^2MC-8FX$ .

### ■ Instruction Overview of F<sup>2</sup>MC-8FX

In  $F^2MC$ -8FX, there are 140 kinds of one byte machine instructions (as the map, 256 bytes), and the instruction code is composed of the instruction and the operand following it.

Figure E-1 shows the correspondence of the instruction code and the instruction map.



Figure E-1 Instruction Code and Instruction Map

- The instruction is classified into following four types; forwarding system, operation system, branch system and others.
- There are various methods of addressing, and ten kinds of addressing can be selected by the selection and the operand specification of the instruction.
- This provides with the bit operation instruction, and can operate the read modification write.
- There is an instruction that directs special operation.

### Explanation of Display Sign of Instruction

Table E-1 shows the explanation of the sign used by explaining the instruction code of this APPENDIX E.

Table E-1 Explanation of Sign in Instruction Table

Sign	Signification
dir	Direct address (8-bit length)
off	Offset (8-bit length)
ext	Extended address (16-bit length)
#vct	Vector table number (3-bit length)
#d8	Immediate data (8-bit length)
#d16	Immediate data (16-bit length)
dir:b	Bit direct address (8-bit length: 3-bit length)
rel	Branch relative address (8-bit length)
@	Register indirect (Example: @A, @IX, @EP)
А	Accumulator (Whether 8- bit length or 16- bit length is decided by the instruction used.)
AH	Upper 8-bit of accumulator (8-bit length)
AL	Lower 8-bit of accumulator (8-bit length)
Т	Temporary accumulator (Whether 8- bit length or 16- bit length is decided by the instruction used.)
TH	Upper 8-bit of temporary accumulator (8-bit length)
TL	Lower 8-bit of temporary accumulator (8-bit length)
IX	Index register (16-bit length)
EP	Extra pointer (16-bit length)
PC	Program counter (16-bit length)
SP	Stack pointer (16-bit length)
PS	Program status (16-bit length)
dr	Either of accumulator or index register (16-bit length)
CCR	Condition code register (8-bit length)
RP	Register bank pointer (5-bit length)
DP	Direct bank pointer (3-bit length)
Ri	General-purpose register (8-bit length, $i = 0$ to 7)
х	This shows that x is immediate data. (Whether 8- bit length or 16- bit length is decided by the instruction used.)
(x)	This shows that contents of x are objects of the access. (Whether 8- bit length or 16- bit length is decided by the instruction used.)
((x))	This shows that the address that contents of x show is an object of the access. (Whether 8- bit length or 16- bit length is decided by the instruction used.)

## Explanation of Item in Instruction Table

Item	Description
MNEMONIC	It shows the assembly description of the instruction.
~	It shows the number of cycles of the instruction. One instruction cycle is a machine cycle. Note: The number of cycles of the instruction can be delayed by 1 cycle by the immediately preceding instruction. Moreover, the number of cycles of the instruction might be extended in the access to the I/O area.
#	It shows the number of bytes for the instruction.
Operation	It shows the operations for the instruction.
TL, TH, AH	<ul> <li>They show the change (auto forwarding from A to T) in the content when each TL, TH, and AH instruction is executed. The sign in the column indicates the followings respectively.</li> <li>-: No change</li> <li>dH: upper 8 bits of the data described in operation.</li> <li>AL and AH: the contents become those of the immediately preceding instruction's AL and AH.</li> <li>00: Become 00</li> </ul>
N, Z, V, C	They show the instruction into which the corresponding flag is changed respectively. The sign in the column shows the followings respectively. • -: No change • +: Change • R: Become "0" • S: Become "1"
OP CODE	It shows the code of the instruction. When a pertinent instruction occupies two or more codes, it follows the following description rules. [Example] 48 to 4F: This shows 48, 494F.

 Table E-2 Explanation of Item in Instruction Table

# E.1 Addressing

F<sup>2</sup>MC-8FX has the following ten types of addressings:

- Direct addressing
- Extended addressing
- Bit direct addressing
- Index addressing
- Pointer addressing
- · General-purpose register addressing
- Immediate addressing
- Vector addressing
- Relative addressing
- Inherent addressing

### Explanation of Addressing

• Direct addressing

This is used when accessing the direct area of  $"0000_{\text{H}}"$  to  $"047F_{\text{H}}"$  with addressing indicated "dir" in instruction table. In this addressing, when the operand address is  $"00_{\text{H}}"$  to  $"7F_{\text{H}}"$ , it is accessed into  $"0000_{\text{H}}"$  to  $"007F_{\text{H}}"$ . Moreover, when the operand address is  $"80_{\text{H}}"$  to "FF<sub>H</sub>", the access can be mapped in  $"0080_{\text{H}}"$  to  $"047F_{\text{H}}"$  by setting of direct bank pointer DP. Figure E.1-1 shows an example.

### Figure E.1-1 Example of Direct Addressing



### • Extended addressing

This is used when the area of the entire 64 K bytes is accessed by addressing shown "ext" in the instruction table. In this addressing, the first operand specifies one high rank byte of the address and the second operand specifies one subordinate position byte of the address.

Figure E.1-2 shows an example.





### Bit direct addressing

This is used when accessing the direct area of " $0000_{\text{H}}$ " to " $047F_{\text{H}}$ " in bit unit with addressing indicated "dir:b" in instruction table. In this addressing, when the operand address is " $00_{\text{H}}$ " to " $7F_{\text{H}}$ ", it is accessed into " $0000_{\text{H}}$ " to " $007F_{\text{H}}$ ". Moreover, when the operand address is " $80_{\text{H}}$ " to " $FF_{\text{H}}$ ", the access can be mapped in " $0080_{\text{H}}$ " to " $047F_{\text{H}}$ " by setting of direct bank pointer DP. The position of the bit in the specified address is specified by the values of the instruction code of three subordinate position bits.

Figure E.1-3 shows an example.

### Figure E.1-3 Example of Bit Direct Addressing



### Index addressing

This is used when the area of the entire 64 K bytes is accessed by addressing shown "@IX+off" in the instruction table. In this addressing, the content of the first operand is sign extended and added to IX (index register) to the resulting address. Figure E.1-4 shows an example.





### Pointer addressing

This is used when the area of the entire 64 K bytes is accessed by addressing shown "@EP" in the instruction table. In this addressing, the content of EP (extra pointer) is assumed to be an address. Figure E.1-5 shows an example.

Figure E.1-5	Example	of Pointer	Addressing
--------------	---------	------------	------------



### General-purpose register addressing

This is used when accessing the register bank in general-purpose register area with the addressing shown "Ri" in instruction table. In this addressing, fix one high rank byte of the address to "01" and create one subordinate position byte from the contents of RP (register bank pointer) and three subordinate bits of the operation code to access to this address. Figure E.1-6 shows an example.

Figure E.1-6 Example of General-purpose Register Addressing						
$\begin{array}{c c} MOV \ A, \ R \underline{6} \\ RP \ \hline 0 \ 1 \ 0 \ 1 \ 0 \\ \hline \end{array} \xrightarrow{V} \qquad 0 \ 1 \ \underline{5 \ 6H}  \hline A \ BH \end{array} \begin{array}{c} A \ BH \end{array}$						

### Immediate addressing

This is used when immediate data is needed in addressing shown "#d8" in the instruction table. In this addressing, the operand becomes immediate data as it is. The specification of byte/word depends on the operation code. Figure E.1-7 shows an example.

### Figure E.1-7 Example of Immediate Addressing



### Vector addressing

This is used when branching to the subroutine address registered in the table with the addressing shown "#vct" in the instruction table. In this addressing, information on "#vct" is contained in the operation code, and the address of the table is created using the combinations shown in Table E.1-1.

#vct	Vector table address (jump destination high-ranking address: subordinate address)
0	FFC0 <sub>H</sub> : FFC1 <sub>H</sub>
1	FFC2 <sub>H</sub> : FFC3 <sub>H</sub>
2	FFC4 <sub>H</sub> : FFC5 <sub>H</sub>
3	FFC6 <sub>H</sub> : FFC7 <sub>H</sub>
4	FFC8 <sub>H</sub> : FFC9 <sub>H</sub>
5	FFCA <sub>H</sub> : FFCB <sub>H</sub>
6	$FFCC_{H} : FFCD_{H}$
7	FFCE <sub>H</sub> : FFCF <sub>H</sub>

Figure E.1-8 shows an example.





### Relative addressing

This is used when branching to the area in 128 bytes before and behind PC (program counter) with the addressing shown "rel" in the instruction table. In this addressing, add the content of the operand to PC with the sign and store the result in PC. Figure E.1-9 shows an example.

Figure E.1-9 Example of Relative Addressing				
BNE <u>FEH</u> Old PC <u>9 A B C</u> H → +	9ABCH + FFFEH > New PC 9 A B AH			

In this example, by jumping to the address where the operation code of BNE is stored, it results in an infinite loop.

### Inherent addressing

This is used when doing the operation decided by the operation code with the addressing that does not have the operand in the instruction table. In this addressing, the operation depends on each instruction. Figure E.1-10 shows an example.

### Figure E.1-10 Example of Inherent Addressing

NOP			
Old PC	9 А В Сн	→ New PC 9 A B	Dн

### E.2 Special Instruction

This section explains special instructions other than the addressings.

### Special Instruction

#### JMP @A

This instruction is to branch the content of A (accumulator) to PC (program counter) as an address. N pieces of the jump destination is arranged on the table, and one of the contents is selected and transferred to A. N branch processing can be done by executing this instruction.

Figure E.2-1 shows a summary of the instruction.

	(Before executing) А 1234н	(After executing) A 1234H	
0	Id PC XXXXH	→ New PC 1 2 3 4H	

Figure E.2-1 JMP @A

#### MOVW A, PC

This instruction works as the opposite of "JMP @A". That is, it stores the content of PC to A. When you have executed this instruction in the main routine and set it to call a specific subroutine, you can make sure that the content of A is the specified value in the subroutine. Also, you can identify that the branch is not from the part that cannot be expected, and use it for the reckless driving judgment.

Figure E.2-2 shows a summary of the instruction.

Figure E.2-2 MOVW A, PC

(Before executing)	(After executing)
A XXXXH	A 1234H
Old PC 1 2 3 3H	New PC 1234H

When this instruction is executed, the content of A reaches the same value as the address where the following instruction is stored, rather than the address where operation code of this instruction is stored. Therefore, in Figure E.2-2, the value " $1234_{\rm H}$ " stored in A corresponds to the address where the following operation code of "MOVW A, PC" is stored.

### MULU A

This instruction performs an unsigned multiplication of AL (lower 8-bit of the accumulator) and TL (lower 8-bit of the temporary accumulator), and stores the 16-bit result in A. The contents of T (temporary accumulator) do not change. The contents of AH (higher 8-bit of the accumulator) and TH (higher 8-bit of the temporary accumulator) before execution of the instruction are not used for the operation. The instruction does not change the flags, and therefore care must be taken when a branch may occur depending on the result of a multiplication.
Figure E.2-3 shows a summary of the instruction.

Figure E.2-3 MULU A

(Befor	e executing)	(After executing)
A 5		А 1860н
Т 1	1 2 3 4н	Т 1234н

#### DIVU A

This instruction divides the 16-bit value in T by the unsigned 16-bit value in A, and stores the 16-bit result and the 16-bit remainder in A and T, respectively. When the value in A before execution of instruction is "0", the Z flag becomes "1" to indicate zero-division is executed. The instruction does not change other flags, and therefore care must be taken when a branch may occur depending on the result of a division.

Figure E.2-4 shows a summary of the instruction.

Figure E.2-4 DIVU A

(Before executing)	(After executing)
А 1234н	А 0004н
Т 5678н	Т 0 D A 8н

#### • XCHW A, PC

This instruction swaps the contents of A and PC, resulting in a branch to the address contained in A before execution of the instruction. After the instruction is executed, A becomes the address that follows the address where the operation code of "XCHW A, PC" is stored. This instruction is effective especially when it is used in the main routine to specify a table for use in a subroutine.

Figure E.2-5 shows a summary of the instruction.

Figure E.2-5 XCHW A, PC

(Before executing) A $5678H$	(After executing) A 1235H
PC 1234H P	>C 5678н

When this instruction is executed, the content of A reaches the same value as the address where the following instruction is stored, rather than the address where operation code of this instruction is stored. Therefore, in Figure E.2-5, the value " $1235_{H}$ " stored in A corresponds to the address where the following operation code of "XCHW A, PC" is stored. This is why " $1235_{H}$ " is stored instead of " $1234_{H}$ ".

Figure E.2-6 shows an assembler language example.

	i igui e Liz e i	stample el elenig ;		
(Main ro	utine)	(Subroutine	)	
MOVW XCHW DB MOVW	A, #PUTSUB A, PC 'PUT OUT DATA', EOL A, 1234H	→ PUTSUB PTS1	XCHW A, EP PUSHW A MOV A, @EP INCW EP MOV IO, A <	_ Output table data here



#### CALLV #vct

This instruction is used to branch to a subroutine address stored in the vector table. The instruction saves the return address (contents of PC) in the location at the address contained in SP (stack pointer), and uses vector addressing to cause a branch to the address stored in the vector table. Because CALLV #vct is a 1-byte instruction, the use of this instruction for frequently used subroutines can reduce the entire program size.

Figure E.2-7 shows a summary of the instruction.





After the CALLV #vct instruction is executed, the contents of PC saved on the stack area are the address of the operation code of the next instruction, rather than the address of the operation code of CALLV #vct. Accordingly, Figure E.2-7 shows that the value saved in the stack  $(1232_{\rm H} \text{ and } 1233_{\rm H})$  is 5679<sub>H</sub>, which is the address of the operation code of the instruction that follows "CALLV #vct" (return address).

Vector use	Vector table address							
(call instruction)	Upper	Lower						
CALLV #7	FFCE <sub>H</sub>	FFCF <sub>H</sub>						
CALLV #6	FFCC <sub>H</sub>	FFCD <sub>H</sub>						
CALLV #5	FFCA <sub>H</sub>	FFCB <sub>H</sub>						
CALLV #4	FFC8 <sub>H</sub>	FFC9 <sub>H</sub>						
CALLV #3	FFC6 <sub>H</sub>	FFC7 <sub>H</sub>						
CALLV #2	FFC4 <sub>H</sub>	FFC5 <sub>H</sub>						
CALLV #1	FFC2 <sub>H</sub>	FFC3 <sub>H</sub>						
CALLV #0	FFC0 <sub>H</sub>	FFC1 <sub>H</sub>						

# E.3 Bit Manipulation Instructions (SETB, CLRB)

# Some peripheral function registers include bits that are read differently than usual by a bit manipulation instruction.

#### ■ Read-modify-write Operation

By using these bit manipulation instructions, you can set only the specified bit in a register or RAM location to "1" (SETB) or clear to "0" (CLRB). However, as the CPU operates data in 8-bit units, the actual operation (read-modify-write operation) involves a sequence of steps: 8-bit data is read, the specified bit is changed, and the data is written back to the location at the original address.

Table E.3-1 shows bus operation for bit manipulation instructions.

Table E.3-1 Bus Operation for Bit Manipulation Instructions

CODE	MNEMONIC	~	Cycle	Address bus	Data bus	RD	WR	RMW
A0 to A7 A8 to AF	CLRB dir:b SETB dir:b	4	1 2 3 4	N+2 dir address dir address N+3	Next instruction Data Data Instruction after next	1 1 0 1	0 0 1 0	1 1 0 0

#### Read Destination on the Execution of Bit Manipulation Instructions

For some I/O ports and the interrupt request flag bits, the read destination differs between a normal read operation and a read-modify-write operation.

#### • I/O ports (during a bit manipulation)

From some I/O ports, an I/O pin value is read during a normal read operation, while a port data register value is read during a bit manipulation. This prevents the other port data register bits from being changed accidentally, regardless of the I/O directions and states of the pins.

#### Interrupt request flag bits (during a bit manipulation)

An interrupt request flag bit functions as a flag bit indicating whether an interrupt request exists during a normal read operation, however, "1" is always read from this bit during a bit manipulation. This prevents the flag from being cleared accidentally by writing the value "0" to the interrupt request flag bit when manipulating another bit.

# E.4 F<sup>2</sup>MC-8FX Instructions

## Table E.4-1 to Table E.4-4 show the instructions used by the $F^2MC-8FX$ .

#### ■ Transfer Instructions

#### Table E.4-1 Transfer Instructions

No.	N	INEMONIC	~	#	Operation	TL	TH	AH	Ν	Ζ	V	С	OPCODE
1	MOV	dir, A	3	2	$(\operatorname{dir}) \leftarrow (A)$	-	-	-	-	-	-	-	45
2	MOV	@IX + off, A	3	2	$((IX) + off) \leftarrow (A)$	-	-	-	-	-	-	-	46
3	MOV	ext, A	4	3	$(\text{ext}) \leftarrow (A)$	-	-	-	-	-	-	-	61
4	MOV	@EP, A	2	1	$((EP)) \leftarrow (A)$	-	-	-	-	-	-	-	47
5	MOV	Ri, A	2	1	$(Ri) \leftarrow (A)$	-	-	-	-	-	-	-	48 to 4F
6	MOV	A, #d8	2	2	$(A) \leftarrow d8$	AL	-	-	+	+	-	-	04
7	MOV	A, dir	3	2	$(A) \leftarrow (dir)$	AL	-	-	+	+	-	-	05
8	MOV	A, @IX + off	3	2	$(A) \leftarrow ((IX) - off)$	AL	-	-	+	+	-	-	06
9	MOV	A, ext	4	3	$(A) \leftarrow (ext)$	AL	-	-	+	+	-	-	60
10	MOV	A, @A	2	1	$(A) \leftarrow ((A))$	AL	-	-	+	+	-	-	92
11	MOV	A, @EP	2	1	$(A) \leftarrow ((EP))$	AL	-	-	+	+	1	-	07
12	MOV	A, Ri	2	1	$(A) \leftarrow (Ri)$	AL	-	-	-	+	-	-	08 to 0F
13	MOV	dir, #d8	4	3	$(dir) \leftarrow d8$	-	-	-	-	-	-	-	85
14	MOV	@IX + off, #d8	4	3	$((IX) + off) \leftarrow d8$	-	-	-	-	-	-	-	86
15	MOV	@EP, #d8	3	2	( (EP) ) ←d8	-	-	-	-	-	-	-	87
16	MOV	Ri, #d8	3	2	$(Ri) \leftarrow d8$	-	-	-	-	-	-	-	88 to 8F
17	MOVW	dir, A	4	2	$(\operatorname{dir}) \leftarrow (\operatorname{AH}), (\operatorname{dir} + 1) \leftarrow (\operatorname{AL})$	-	-	-	-	-	-	-	D5
18	MOVW	@IX + off, A	4	2	$((IX) + off) \leftarrow (AH), ((IX) + off + 1) \leftarrow (AL)$	-	-	-	-	-	-	-	D6
19	MOVW	ext, A	5	3	$(ext) \leftarrow (AH), (ext + 1) \leftarrow (AL)$	-	-	-	-	-	-	-	D4
20	MOVW	@EP, A	3	1	$((EP)) \leftarrow (AH), ((EP) + 1) \leftarrow (AL)$	-	-	-	-	-	-	-	D7
21	MOVW	EP, A	1	1	$(EP) \leftarrow (A)$	-	-	-	-	1	1	-	E3
22	MOVW	A, #d16	3	3	$(A) \leftarrow d16$	AL	AH	dH	+	+	-	-	E4
23	MOVW	A, dir	4	2	$(AH) \leftarrow (dir), (AL) \leftarrow (dir - 1)$	AL	AH	dH	+	+	-	-	C5
24	MOVW	A, @IX + off	4	2	$(AH) \leftarrow ((IX) + off), (AL) \leftarrow ((IX) + off-1)$	AL	AH	dH	-	+	-	-	C6
25	MOVW	A, ext	5	3	$(AH) \leftarrow (ext), (AL) \leftarrow (ext - 1)$	AL	AH	dH	+	+	-	-	C4
26	MOVW	A, @A	3	1	$(AH) \leftarrow ((A)), (AL) \leftarrow ((A) + 1)$	AL	AH	dH	+	+	-	-	93
27	MOVW	A, @EP	3	1	$(AH) \leftarrow ((EP)), (AL) \leftarrow ((EP) + 1)$	AL	AH	dH	-	+	-	-	C7
28	MOVW	A, EP	1	1	$(A) \leftarrow (EP)$	-	-	dH	-	-	-	-	F3
29	MOVW	EP, #d16	3	3	$(EP) \leftarrow d16$	-	-	-	-	-	-	-	E7
30	MOVW	IX, A	1	1	$(IX) \leftarrow (A)$	-	-	-	-	-	-	-	E2
31	MOVW	A, IX	1	1	$(A) \leftarrow (IX)$	-	-	dH	-	-	-	-	F2
32	MOVW	SP, A	1	1	$(SP) \leftarrow (A)$	-	-	-	-	-	-	-	E1
33	MOVW	A, SP	1	1	$(A) \leftarrow (SP)$	-	-	dH	-	-	-	-	F1
34	MOV	@A, T	2	1	$((A)) \leftarrow (T)$	-	-	-	-	-	-	-	82
35	MOVW	@A, T	3	1	$((A)) \leftarrow (TH), ((A) - 1) \leftarrow (TL)$	-	-	-	-	-	-	-	83
L													
36	MOVW	IX, #d16	3	3	$(IX) \leftarrow d16$	-	-	-	-	-	-	-	E6
37	MOVW	A, PS	1	1	$(A) \leftarrow (PS)$	-	-	dH	-	-	-	-	70
38	MOVW	PS, A	1	1	$(PS) \leftarrow (A)$	-	-	-	+	+	-	+	71
39	MOVW	SP, #d16	3	3	(SP) ←d16	-	-	-	-	-	-	-	E5
40	SWAP		1	1	$(AH) \leftarrow \rightarrow (AL)$	-	-	AL	-	-	-	-	10
41	SETB	dir:b	4	2	$(dir): b \leftarrow 1$	-	-	-	-	-	-	-	A8 to AF
42	CLRB	dir:b	4	2	(dir) : b←0	-	-	-	-	-	-	-	A0 to A7
43	XCH	A, T	1	1	$(AL) \leftarrow \rightarrow (TL)$	AL	-	-	-	-	-	-	42
44	XCHW	A, T	1	1	$(A) \longleftrightarrow (I')$	AL	AH	dH	-	-	-	-	43
45	XCHW	A, EP	1	1	$(A) \leftarrow \rightarrow (EP)$	-	-	dH	-	-	-	-	F7
L													
46	XCHW	A, IX	1	1	$(A) \longleftrightarrow (IX)$	-	-	dH	-	-	-	-	F6
47	XCHW	A, SP	1	1	$(A) \longleftrightarrow (SP)$	-	-	dH	-	-	-	-	F5
48	MOVW	A, PC	2	1	$(A) \leftarrow (PC)$	-	-	dH	-	-	-	-	F0

Note:

In automatic transfer to T during byte transfer to A, AL is transferred to TL. If an instruction has plural operands, they are saved in the order indicated by MNEMONIC.

## ■ Arithmetic Operation Instructions

Table E.4-2	Arithmetic	Operation	Instruction	(1	/ 2	2)
-------------	------------	-----------	-------------	----	-----	----

No.	MNEMONIC	~	#	Operation	TL	TH	AH	Ν	Ζ	V	С	OPCODE
1	ADDC A, Ri	2	1	$(A) \leftarrow (A) + (Ri) + C$	-	-	-	+	+	+	+	28 to 2F
2	ADDC A, #d8	2	2	$(A) \leftarrow (A) + d8 + C$	-	-	-	+	+	+	+	24
3	ADDC A, dir	3	2	$(A) \leftarrow (A) + (dir) + C$	-	-	-	+	+	+	+	25
4	ADDC A, @IX + o	off 3	2	$(A) \leftarrow (A) + ((IX) + off) + C$	-	-	-	+	+	+	+	26
5	ADDC A, @EP	2	1	$(A) \leftarrow (A) + ((EP)) + C$	-	-	-	+	+	+	+	27
	,											
6	ADDCW A	1	1	$(A) \leftarrow (A) + (T) + C$	-	-	dH	+	+	+	+	23
7	ADDC A	1	1	$(AL) \leftarrow (AL) + (TL) + C$	-	-	-	+	+	+	+	22
8	SUBC A. Ri	2	1	$(A) \leftarrow (A) - (Ri) - C$	-	-	-	+	+	+	+	38 to 3F
9	SUBC A. #d8	2	2	$(A) \leftarrow (A) - d8 - C$	-	-	-	+	+	+	+	34
10	SUBC A dir	3	2	$(A) \leftarrow (A) - (dir) - C$	-	-	-	+	+	+	+	35
			-					-				
11	SUBC A $@IX + c$	off 3	2	$(A) \leftarrow (A) - ((IX) + off) - C$	-	-	-	+	+	+	+	36
12	SUBC A @FP	2	1	$(A) \leftarrow (A) - ((FP)) - C$	-	-	-	+	+	+	+	37
13	SUBCW A	1	1	$(A) \leftarrow (T) - (A) - C$	-	-	dH	+	+	+	+	33
14	SUBC A	1	1	$(\Lambda I) \leftarrow (\Pi I) = (\Lambda I) = C$	_	_	un		-		- -	32
15	INC Pi	3	1	$(\mathbf{R}) \leftarrow (\mathbf{R}) + 1$	_	_	_			-	'	C8 to CE
15	INC KI	5	1	$(\mathbf{R}) \leftarrow (\mathbf{R}) + 1$	-	-		т	т	т	-	C8 10 C1
16	INCW ED	1	1	$(ED) \leftarrow (ED) + 1$								C2
10	INCW EF	1	1	$(\mathbf{E}\mathbf{F}) \leftarrow (\mathbf{E}\mathbf{F}) + 1$	-	-	-	-	-	-	-	C3
1/	INCW IA	1	1	$(IX) \leftarrow (IX) + 1$	-	-	-	-	-	-	-	C2
18	INCW A	1	1	$(A) \leftarrow (A) + 1$	-	-	đН	+	+	-	-	D8 4: DE
19	DEC KI	3	1	$(\mathbf{K}\mathbf{I}) \leftarrow (\mathbf{K}\mathbf{I}) - \mathbf{I}$	-	-	-	+	+	+	-	D8 to DF
20	DECW EP	1	1	$(EP) \leftarrow (EP) - 1$	-	-	-	-	-	-	-	D3
1	DEGUL W											5.0
21	DECW IX	1	1	$(IX) \leftarrow (IX) - 1$	-	-	-	-	-	-	-	D2
22	DECW A	1	1	$(A) \leftarrow (A) - 1$	-	-	dH	+	+	-	-	D0
23	MULU A	8	1	$(A) \leftarrow (AL) \times (TL)$	-	-	dH	-	-	-	-	01
24	DIVU A	17	1	$(A) \leftarrow (T) / (A), MOD \rightarrow (T)$	dL	dH	dH	-	+	-	-	11
25	ANDW A	1	1	$(A) \leftarrow (A) \land (T)$	-	-	dH	+	+	R	-	63
26	ORW A	1	1	$(A) \leftarrow (A) \lor (T)$	-	-	dH	+	+	R	-	73
27	XORW A	1	1	$(A) \leftarrow (A) \forall (T)$	-	-	dH	+	+	R	-	53
28	CMP A	1	1	(TL) - (AL)	-	-	-	+	+	+	+	12
29	CMPW A	1	1	(T) - (A)	-	-	-	+	+	+	+	13
30	RORC A	1	1	$\rightarrow C \rightarrow A$	-	-	-	+	+	-	+	0302
31	ROLCA	1	1		-	-	-	+	+	-	+	
32	CMP A, #d8	2	2	(A) - d8	-	-	-	+	+	+	+	14
33	CMP A, dir	3	2	(A) - (dir)	-	-	-	+	+	+	+	15
34	CMP A, @EP	2	1	(A) - ( (EP) )	-	-	-	+	+	+	+	17
35	CMP A, @IX + c	off 3	2	(A) - ((IX) + off)	-	-	-	+	+	+	+	16
<u> </u>			1		1							
36	CMP A, Ri	2	1	(A) - (Ri)	-	-	-	+	+	+	+	18 to 1F
37	DAA	1	1	decimaladjustforaddition	-	-	-	+	+	+	+	84
38	DAS	1	1	decimaladjustforsubtraction	-	-	-	+	+	+	+	94
39	XOR A	1	1	$(A) \leftarrow (AL) \lor (TL)$	-	-	-	+	+	R	-	52
40	XOR A. #d8	2	2	$(A) \leftarrow (AL) \lor d8$	-	-	-	+	+	R	-	54
			+						<u> </u>	<u> </u>		54
41	XOR A dir	3	2	$(A) \leftarrow (AL) \lor (dir)$	-	-	-	+	+	R	-	55
42	XOR A @FP	2	1	$(A) \leftarrow (AL) \lor ((EP))$	-	-	-	+	+	R	-	57
43	$XOR$ A $@IY \pm c$	off 3	2	$(A) \leftarrow (AL) \lor ((IX) + off)$	-	-	_	+	+	R	-	56
44	XOR A Ri	···· 5	1	$(A) \leftarrow (AL) \lor (Ri)$	-	_		-	- -	R	_	58 to 5F
44	AND A	2	1	$(\Delta) \leftarrow (\Delta I) \land (TI)$	<u> </u>	<u> </u>		+	+	P	<u> </u>	50 10 JF
45		1	-		-	<u> </u>		C.	г	A	Ļ	02
		1	1		1							

No.		MNEMONIC	~	#	Operation	TL	TH	AH	Ν	Ζ	V	С	OPCODE
46	AND	A, #d8	2	2	$(A) \leftarrow (AL) \land d8$	-	-	-	+	+	R	-	64
47	AND	A, dir	3	2	$(A) \leftarrow (AL) \land (dir)$	-	-	-	+	+	R	1	65
48	AND	A, @EP	2	1	$(A) \leftarrow (AL) \land ((EP))$	-	-	-	+	+	R	1	67
49	AND	A, @IX + off	3	2	$(A) \leftarrow (AL) \land ((IX) + off)$	-	-	-	+	+	R	1	66
50	AND	A, Ri	2	1	$(A) \leftarrow (AL) \land (Ri)$	-	-	-	+	+	R	1	68 to 6F
51	OR	А	1	1	$(A) \leftarrow (AL) \lor (TL)$	-	-	-	+	+	R	i.	72
52	OR	A, #d8	2	2	$(A) \leftarrow (AL) \lor d8$	-	-	-	+	+	R	1	74
53	OR	A, dir	3	2	$(A) \leftarrow (AL) \lor (dir)$	-	-	-	+	+	R	1	75
54	OR	A, @EP	2	1	$(A) \leftarrow (AL) \lor ((EP))$	-	-	-	+	+	R	1	77
55	OR	A, @IX + off	3	2	$(A) \leftarrow (AL) \lor ((IX) + off)$	-	-	-	+	+	R	1	76
56	OR	A, Ri	2	1	$(A) \leftarrow (AL) \lor (Ri)$	-	-	-	+	+	R	i.	78 to 7F
57	CMP	dir, #d8	4	3	(dir) - d8	-	-	-	+	+	+	+	95
58	CMP	@EP, #d8	3	2	( (EP) ) - d8	-	-	-	+	+	+	+	97
59	CMP	@IX + off, #d8	4	3	( (IX) + off) - d8	-	-	-	+	+	+	+	96
60	CMP	Ri, #d8	3	2	(Ri) - d8	-	-	-	+	+	+	+	98 to 9F
61	INCW	SP	1	1	$(SP) \leftarrow (SP) + 1$	-	-	-	-	-	-	-	C1
62	DECW	SP	1	1	$(SP) \leftarrow (SP) - 1$	-	-	-	-	-	-	-	D1

## Table E.4-2 Arithmetic Operation Instruction (2 / 2)

## Branch Instructions

#### Table E.4-3 Branch Instructions

No.	М	NEMONIC	~	#	Operation	TL	TH	AH	Ν	Ζ	V	С	OPCODE
1	BZ/BEQ	rel(at branch)	4	2	$ifZ = 1thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	FD
	BZ/BEQ	rel(at no branch)	2										
2	BNZ/BNE	rel(at branch)	4	2	$ifZ = 0thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	FC
	BNZ/BNE	rel(at no branch)	2										
3	BC/BLO	rel(at branch)	4	2	$ifC = 1thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	F9
	BC/BLO	rel(at no branch)	2										
4	BNC/BHS	rel(at branch)	4	2	$ifC = 0thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	F8
	BNC/BHS	rel(at no branch)	2										
5	BN	rel(at branch)	4	2	$ifN = 1thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	FB
	BN	rel(at no branch)	2										
6	BP	rel(at branch)	4	2	$ifN = 0thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	FA
	BP	rel(at no branch)	2										
7	BLT	rel(at branch)	4	2	$ifV \forall N = 1 then PC \leftarrow PC + rel$	-	-	-	-	-	-	-	FF
	BLT	rel(at no branch)	2										
8	BGE	rel(at branch)	4	2	$ifV \forall N = 0thenPC \leftarrow PC + rel$	-	-	-	-	-	-	-	FE
	BGE	rel(at no branch)	2										
9	BBC	dir : b, rel	5	3	if (dir : b) = 0thenPC $\leftarrow$ PC + rel	-	-	-	-	+	-	-	B0 to B7
10	BBS	dir : b, rel	5	3	if (dir : b) = 1thenPC $\leftarrow$ PC + rel	-	-	-	-	+	-	-	B8 to BF
11	JMP	@A	3	1	$(PC) \leftarrow (A)$	-	-	-	-	-	-	-	E0
12	JMP	ext	4	3	$(PC) \leftarrow ext$	-	-	-	-	-	-	-	21
13	CALLV	#vct	7	1	vectorcall	-	-	-	-	-	-	-	E8 to EF
14	CALL	ext	6	3	subroutinecall	-	-	-	-	-	-	-	31
15	XCHW	A, PC	3	1	$(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$	-	-	dH	-	-	-	-	F4
16	RET		6	1	returnfromsubroutine	-	-	-	-	-	-	-	20
17	RETI		8	1	returnfrominterrupt	-	-	-		res	tore		30

## Other Instructions

#### Table E.4-4 Other Instructions

No.	MNEMONIC	~	#	Operation	TL	TH	AH	Ν	Ζ	V	С	OPCODE
1	PUSHW A	4	1	$((SP))\leftarrow(A), (SP)\leftarrow(SP) - 2$	-	i.	-	-	-	-	-	40
2	POPW A	3	1	$(A) \leftarrow ((SP)), (SP) \leftarrow (SP) + 2$	1	ı.	dH	-	-	-	-	50
3	PUSHW IX	4	1	$((SP))\leftarrow(IX), (SP)\leftarrow(SP) - 2$	1	ı.	-	-	-	-	-	41
4	POPW IX	3	1	$(IX) \leftarrow ((SP)), (SP) \leftarrow (SP) + 2$	1	ı.	-	-	-	-	-	51
5	NOP	1	1	No operation	1	ı.	-	-	-	-	-	00
6	CLRC	1	1	(C)←0	i.	ı.	-	-	-	-	R	81
7	SETC	1	1	(C)←1	1	ı.	-	-	-	-	S	91
8	CLRI	1	1	(I)←0	-	1	-	-	-	-	-	80
9	SETI	1	1	(I)←1	-	1	-	-	-	-	-	90

# E.5 Instruction Map

## Table E.5-1 shows the instruction map of $F^2MC-8FX$ .

## ■ Instruction Map

## Table E.5-1 Instruction Map of F<sup>2</sup>MC-8FX

# APPENDIX F Mask Option

## The mask option list of the MB95130/M series is shown in Table F-1.

## Mask Option List

Table F-1 Mask Option List 1

No.	Part number	MB95136M	MB95F133MS/ F133NS MB95F134MS/ F134NS MB95F136MS/ F136NS	MB95F133MW/ F133NW MB95F134MW/ F134NW MB95F136MW/ F136NW	MB95FV100D-103
	Specifying procedure	Setting disabled	Setting disabled	Setting disabled	Setting disabled
1	Clock mode select <ul> <li>Single-system clock mode</li> <li>Dual-system clock mode</li> </ul>	Specify when ordering MASK	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	<ul> <li>Low voltage detection reset*</li> <li>With low voltage detection reset</li> <li>Without low voltage detection reset</li> </ul>	Specify when ordering MASK	Specified by part number	Specified by part number	Change by the switch on MCU board
3	Oscillation stabilization wait time	Fixed to oscillation stabilization wait time of (2 <sup>14</sup> -2) /F <sub>CH</sub>	Fixed to oscilla- tion stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscilla- tion stabilization wait time of $(2^{14}-2)/F_{CH}$	Fixed to oscillation stabilization wait time of (2 <sup>14</sup> -2) /F <sub>CH</sub>

Part number	Clock mode select	Low voltage detection reset		
		No		
	Single - system	Yes		
MD05126M		Yes		
WID95150WI		No		
	Dual - system	Yes		
		Yes		
MB95F133MS		No		
MB95F133NS	Single system	Yes		
MB95F134MS		No		
MB95F134NS	Single - System	Yes		
MB95F136MS	No			
MB95F136NS		Yes		
MB95F133MW		No		
MB95F133NW	Dual sustan	Yes		
MB95F134MW		No		
MB95F134NW	Duai - system	Yes		
MB95F136MW		No		
MB95F136NW		Yes		
		No		
	Single - system	Yes		
MB95EV100D-103	Yes			
1112/51 + 1000-105		No		
	Dual - system	Yes		
		Yes		

# APPENDIX G Writing to Flash Microcontroller Using Parallel Writer

This section describes writing to flash microcontroller using parallel writer.

#### ■ Writing to Flash Microcontroller Using Parallel Writer

#### Table G-1 Parallel Writer and Adaptor

Package	Compatible adaptor model	Parallel writer			
1 ackage	Flash Support Group, Inc.				
FPT-28P-M17	TEF110-95F136HSPF	AF9708 (Ver 02.35G higher) AF9709/B (Ver 02.35G higher)			

Contact

Flash Support Group, Inc. Tel: +81-53-428-8380

#### Sector Configuration

The following diagram shows the addresses corresponding to each sector on accessing using CPU and parallel writer.



#### How to Write

- 1) Set the type code of parallel writer to 17237.
- 2) Load program data to "71000<sub>H</sub> to  $7FFFF_H$ " of parallel writer.
- 3) Write using parallel writer.

#### Numerics

16-bit
16-bit PPG Cycle Setting Buffer Registers
(PCSRH0, PCSRL0)
16-bit PPG Down Counter Registers
(PDCRH0, PDCRL0)
16-bit PPG Duty Setting Buffer Registers
(PDUTH0, PDUTL0)
16-bit PPG Status Control Register, Lower Byte
(PCNTL0)
16-bit PPG Status Control Register, Upper Byte
(PCNTH0)
16-bit PPG Timer
Block Diagram of 16-bit PPG Timer
Block Diagrams of Pins Related
to 16-bit PPG 262
Channels of 16-bit PPG Timer
Interrupts of 16-bit PPG Timer
Operation of 16-bit PPG Mode
Pins of 16-bit PPG Timer
Precautions when Using 16-bit PPG Timer 276
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer
Registers of 16-bit PPG Timer
Sample Programs for 16-bit PPG Timer
Setting 16-bit PPG Mode
16-bit Data
Placement of 16-bit Data in Memory 39
16-bit PPG Cycle Setting Buffer Registers
16 bit PPG Cycle Setting Buffer Registers
(PCSRH0 PCSRI 0) 265
(I CSKIIO, I CSKEO)
16-bit PPG Down Counter Registers
16-bit PPG Down Counter Registers
(PDCRH0, PDCRL0)
16-bit PPG Duty Setting Buffer Registers
16-bit PPG Duty Setting Buffer Registers
(PDUTH0, PDUTL0)
16-bit PPG Status Control Register
16-bit PPG Status Control Register, Lower Byte
(PCNTL0)
16-bit PPG Status Control Register, Upper Byte
(PCNTH0)
256-Kbit Flash Memory
Features of 256-Kbit Flash Memory
Overview of 256-Kbit Flash Memory
Sector Configuration of 256-Kbit Flash
Memory 445
8/10-bit
Block Diagram of 8/10-bit A/D Converter 419

Block Diagram of Pins Related to 8/10-bit A/D
Converter
Interrupts During 8/10-bit A/D Converter
Operation429
List of 8/10-bit A/D Converter Registers423
Notes on Use of 8/10-bit A/D Converter433
Operations of 8/10-bit A/D Converter's Conversion
Function430
Pins of 8/10-bit A/D Converter421
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts429
Sample Programs for 8/10-bit A/D
Converter434
8/10-bit A/D Converter
Block Diagram of 8/10-bit A/D Converter419
Block Diagram of Pins Related to 8/10-bit A/D
Converter422
Interrupts During 8/10-bit A/D Converter
Operation429
List of 8/10-bit A/D Converter Registers423
Notes on Use of 8/10-bit A/D Converter433
Operations of 8/10-bit A/D Converter's Conversion
Function430
Pins of 8/10-bit A/D Converter421
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts
Sample Programs for 8/10-bit A/D
Converter
8/10-bit A/D Converter Control Register
8/10-bit A/D Converter Control Register 1
(ADC1)
8/10-bit A/D Converter Control Register 2
(ADC2)
8/10-bit A/D Converter Data Registers
8/10-bit A/D Converter Data Registers Upper/Lower
(ADDH,ADDL)428
8/10-bit A/D Converter Registers
List of 8/10-bit A/D Converter Registers423
8/16-bit
8/16-bit Compound Timer 00/01 Control Status
Register 0 (T00CR0/T01CR0)197
8/16-bit Compound Timer 00/01 Control Status
Register 1 (T00CR1/T01CR1)200
8/16-bit Compound Timer 00/01 Data Register
(T00DR/T01DR)206
8/16-bit Compound Timer 00/01 Timer Mode Control
Register ch.0 (TMCR0)203
8/10-bit PPG Output Inversion Register
(KEVC)
o/10-Dit PPG Start Register (PPGS)243

8/16-bit PPG Timer 00 Control Register ch.0
(PC00)239
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register
(PPS01/PPS00)241
8/16-bit PPG Timer 00/01 Duty Setup Buffer Register
(PDS01/PDS00)242
8/16-bit PPG Timer 01 Control Register ch.0
(PC01)237
Block Diagram of 8/16-bit Compound
Timer 191
Block Diagram of 8/16-bit PPG231
Block Diagram of Pins Related to 8/16-bit Compound
Timer195
Block Diagram of Pins Related
to 8/16-bit PPG235
Channels of 8/16-bit Compound Timer193
Channels of 8/16-bit PPG233
Interrupts of 8/16-bit PPG245
LIN Synch Field Edge Detection Interrupt (8/16-bit
Compound Timer Interrupt)
Overview of 8/16-bit PPG230
Pins of 8/16-bit PPG234
Pins Related to 8/16-bit Compound Timer
Precautions when Using 8/16-bit Compound
Timer
Precautions when Using 8/16-bit PPG253
Registers and Vector Table Related to Interrupts
of 8/16-bit PPG245
Registers and Vector Tables Related to Interrupts
of 8/16-bit Compound Timer210
Registers of 8/16-bit PPG236
Registers Related to 8/16-bit Compound
Timer 196
Sample Programs for 8/16-bit PPG Timer254

8/16-bit Compound Timer 00/01 Control Status Register
8/16-bit Compound Timer 00/01 Control Status Register 0 (T00CR0/T01CR0)
8/16-bit Compound Timer 00/01 Control Status Register 1 (T00CR1/T01CR1)
8/16-bit Compound Timer 00/01 Data Register 8/16-bit Compound Timer 00/01 Data Register (T00DB/T01DB) 206
8/16-bit Compound Timer 00/01 Timer Mode Control Register
8/16-bit Compound Timer 00/01 Timer Mode Control Register ch.0 (TMCR0)
8/16-bit PPG Output Inversion Register 8/16-bit PPG Output Inversion Register
(REVC)
8/16-bit PPG Start Register 8/16-bit PPG Start Register (PPGS)
8/16-bit PPG Timer 00 Control Register 8/16-bit PPG Timer 00 Control Register ch.0 (PC00)
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register (PPS01/PPS00)241
8/16-bit PPG Timer 00/01 Duty Setup Buffer Register 8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/PDS00)
8/16-bit PPG Timer 01 Control Register 8/16-bit PPG Timer 01 Control Register ch.0
(PC01)
8-DII Operation of 8 bit PBC Independent Mode 247
Operation of 8-bit Prescaler $\pm$ 8-bit PPG
Mode
Setting 8-bit Independent Mode
Setting 8-bit Prescaler + 8-bit PPG Mode

## Α

A/D
8/10-bit A/D Converter Control Register 1 (ADC1)
8/10-bit A/D Converter Control Register 2 (ADC2)
8/10-bit A/D Converter Data Registers Upper/Lower (ADDH,ADDL)
A/D Conversion Functions
Block Diagram of 8/10-bit A/D Converter 419
Block Diagram of Pins Related to 8/10-bit A/D Converter
Interrupts During 8/10-bit A/D Converter
Operation
List of 8/10-bit A/D Converter Registers
Notes on Use of 8/10-bit A/D Converter
Operations of 8/10-bit A/D Converter's Conversion
Function
Operations of A/D Conversion Function
Pins of 8/10-bit A/D Converter
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts
Sample Programs for 8/10-bit A/D
Converter
A/D Conversion Functions 419
A/D Conversion Functions
Operations of A/D Conversion Function
A/D Converter
Block Diagram of 8/10-bit A/D Converter 419 Block Diagram of Pins Related to 8/10-bit A/D
Converter
Interrupts During 8/10-bit A/D Converter
Operation
List of 8/10-bit A/D Converter Registers
Notes on Use of 8/10-bit A/D Converter
Operations of 8/10-bit A/D Converter's Conversion
Function
Pins of 8/10-bit A/D Converter
Converter Interrunts
Sample Programs for 8/10 bit A/D
Converter A34
A/D Converter Registere
A/D COnverter Registers
List of 8/10-bit A/D Converter Registers
ADU 2/10 hit A/D Commenter Control Desister 1
8/10-bit A/D Converter Control Register 1
(ADC1)
(ADC2)
(ADDH,ADDL)
Addressing
Explanation of Addressing 484

Arithmetic Operation	
Arithmetic Operation Instructions49	94
Asynchronous LIN Mode	
Asynchronous LIN Mode Operation	98
Asynchronous Mode	
Asynchronous Mode Operation	90

## В

Baud Rate
Baud Rate Calculation
Baud Rate Setting
Block Diagram of UART/SIO Dedicated Baud Rate
Generator
Channels of UART/SIO Dedicated Baud Rate
Generator
LIN-UART Baud Rate Selection
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1)
Operation of Dedicated Baud Rate Generator
(Reload Counter)
Registers Related to UAR I/SIO Dedicated Baud Rate
Generator
of Each Clock Speed
ULART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR) 346
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR) 345
Baud Pate Concrator Pagister
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1)
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1) 371
Bidirectional Communication
Bidirectional Communication Function 402
Rit 5
One-shot Mode (MDSE of PCNTH0 Register:
bit $5-1$ ) 274
PWM Mode (MDSE of PCNTH Register:
hit 5=0)
Bit Configuration
Bit Configuration of LIN-UART Extended
Communication Control Register
(ECCR)
Bit Configuration of LIN-UART Extended Status
Control Register (ESCR)
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1)
Bit Manipulation Instructions
Read Destination on the Execution of Bit
Manipulation Instructions
Bits Result Information Bits
Bits Result Information Bits35

Block Diagram
Block Diagram of 16-bit PPG Timer
Block Diagram of 8/10-bit A/D Converter419
Block Diagram of 8/16-bit Compound
Timer191
Block Diagram of 8/16-bit PPG231
Block Diagram of All MB95130/M Series8
Block Diagram of External Interrupt
Circuit
Block Diagram of Interrupt Pin Selection
Circuit
Block Diagram of Law voltage Detection Deset
Circuit 430
Block Diagram of Pins Related to 8/10-bit A/D
Converter 422
Block Diagram of Pins Related to 8/16-bit Compound
Timer
Block Diagram of Pins Related
to 8/16-bit PPG235
Block Diagram of Pins Related to External Interrupt
Circuit
Block Diagram of Pins Related
to UART/SIO311
Block Diagram of Port 0 103
Block Diagram of Port 1 108
Block Diagram of Port F 113
Block Diagram of Port G118
Block Diagram of the Clock Controller
Block Diagram of Timebase Timer
Block Diagram of UART/SIO
Block Diagram of UAR1/SIO Dedicated Baud Rate
Black Diagram of Watch Counter 162
Block Diagram of Watch Prescalar 140
Block Diagram of Watchdog Timer 139
Block Diagram of Wild Register Function 177
Block Diagrams of Pins Related
to 16-bit PPG
LIN-UART Block Diagram
Prescaler Block Diagram
Branch
Branch Instructions
BRSR
UART/SIO Dedicated Band Rate Generator Band
Rate Setting Register (BRSR)

## С

Calculation	
Baud Rate Calculation	. 382
Causes	
Table of Interrupt Causes	.476
CCR	
Configuration of Condition Code Register	
(CCR)	35

Channels
Channels of 16-bit PPG Timer 261
Channels of 8/16-bit Compound Timer 193
Channels of 8/16-bit PPG 233
Channels of External Interrupt Circuit
Channels of UART/SIO 309
Channels of UART/SIO Dedicated Baud Rate
Generator
Check
Check That Clock-mode Transition
has been Completed before Setting Standby Mode67
Chip Erase
Erasing Data from Flash Memory
(Chip Erase) 461
Notes on Chip Erasing
Clearing
Clearing Timebase Timer 132
Clearing Watch Prescaler 156
Clock
Block Diagram of the Clock Controller <b>13</b>
Check That Clock mode Transition
has been Completed before Setting Standby
Mode 67
Clock Mode State Transition Diagram 62
Clock Oscillator Circuit 75
Combinations of Clock Mode and Standby
Mode 47
Configuration of System Clock Control Register
(SYCC)
External Clock
Input Clock 78, 126, 140, 150, 164, 192,
232, 260, 308, 342, 356, 420
Operations in Main Clock Mode61
Operations in Main PLL Clock Mode61
Operations in Sub PLL Clock Mode
(on Two-system Clock Product) 61
Oscillation Stabilization Wait Time and Clock Mode/
Standby Mode Transition
Output Clock 78, 126, 150, 342
Overview of Clock Controller 42
Peripheral Resources not Affected
by Clock Mode 45
PLL Clock Oscillation Stabilization Wait Time
Reload Value and Baud Rate of Each Clock Speed
Clock Controller
Block Diagram of the Clock Controller
Overview of Clock Controller
Clock Mode State Transition Diagram
Clock Modes
Combinations of Clock Mode and Standby
Mode
operations in Main Clock Mode

Operations in Main PLL Clock Mode
(on Two-system Clock Product)
Oscillation Stabilization Wait Time and Clock Mode/
Standby Mode Transition
Peripheral Resources not Affected
by Clock Mode
Combinations
Combinations of Clock Mode and Standby
Mode
Command
Command Sequence Table 449
Notes on Issuing Commands
Command Sequence Table
Command Sequence Table 449
Communication
Bidirectional Communication Function 402
Bit Configuration of LIN UART Extended
Communication Control Pagistor
(ECCR) 360
LIN Master/Slave Mode Communication
Euror Function 407
Master/Slave Mode Communication
Function 404
Compara
Wild Degister Address Commons Enchle Degister
who Register Address Compare Enable Register
(WREN) 183
(WREN)

Configuration	
Bit Configuration of LIN-UART Extended	
Communication Control Register	
(FCCR)	360
Bit Configuration of LIN UART Extended State	
Control Register (ESCR)	15 267
Configuration of Condition Code Desister	
	25
(UCK)	30
Configuration of Dedicated Registers	30
Configuration of Direct Bank Pointer (DP)	33
Configuration of General-purpose Registers	37
Configuration of Interrupt Level Setting Registe	ers
(ILR0 to ILR5)	92
Configuration of Memory Space	22
Configuration of Oscillation Stabilization Wait	Time
Setting Register (WAIR)	55
Configuration of PLL Control Register	
(PLLC)	52
Configuration of Register Bank Pointer (RP)	32
Configuration of Reset Source Register	
(RSRR)	86
Configuration of System Clock Control Registe	r
(SYCC)	50
LIN-UART Bit Configuration of Baud Rate Gen	erator
Register (BGR 0/1)	371
Port 0 Configuration	101
Port 1 Configuration	107
Port F Configuration	112
Port G Configuration	117
Sector Configuration	500
Sector Configuration of 256-Khit Elash	
Memory	445
Connection Mathed	
	000
Inter-CPU Connection Method	389
Continuous Mode	
Interval Timer Function	
(Continuous Mode)	188
Operation of Interval Timer Function	
(Continuous Mode)	213
Control Register	
16-bit PPG Status Control Register, Lower Byte	<b>,</b>
(PCNTI 0)	269
16-bit PPG Status Control Register Upper Byte	
(DCNTUO)	267
(I CN III0)	207
(DC00)	220
(PC00)	239
8/16-bit PPG Timer 01 Control Register ch.0	007
(PC01)	237
Bit Configuration of LIN-UART Extended	
Communication Control Register	_
(ECCR)	369
Conversion	
A/D Conversion Functions	418
Operations of 8/10-bit A/D Converter's Converse	sion
Function	430
Operations of A/D Conversion Function	431
•	

#### Counter

16-bit PPG Down Counter Registers	
(PDCRH0, PDCRL0)	264
Block Diagram of Watch Counter	163
Function of Reload Counter	386
Interrupts of Watch Counter	169
Operation of Dedicated Baud Rate Generator	
(Reload Counter)	
Register and Vector Table Related to Interrup	ots of
Watch Counter	169
Registers of Watch Counter	165
Sample Programs for Watch Counter	173
Setup Procedure of Watch Counter	170
Watch Counter	162
Watch Counter Control Register (WCSR)	167
Watch Counter Data Register (WCDR)	166
CPU	
Inter-CPU Connection Method Standby Mode is Also Canceled when the CF	389 YU
Rejects Interrupts.	67

## D

Data Polling Flag
Data Polling Flag (DQ7)453
Dedicated Baud Rate Generator
Block Diagram of UART/SIO Dedicated Baud Rate
Generator
Channels of UART/SIO Dedicated Baud Rate
Generator
Operation of Dedicated Baud Rate Generator
(Reload Counter)
Registers Related to UART/SIO Dedicated Baud Rate
Generator
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR)
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
Dedicated Registers
Configuration of Dedicated Registers
Functions of Dedicated Registers
Description
Operating Description of UART/SIO Operation
Mode 0
Operating Description of UART/SIO Operation
Mode 1
Pin Description11
Details
Details of Programming/Erasing
Flash Memory457
Device
Device Handling Precautions16

#### Е

ECCR
Bit Configuration of LIN-UART Extended
Communication Control Register
(ECCR)
Effect
Effect of Reset on RAM Contents
EIC
External Interrupt Control Register (EIC00) 287
Enable Transmission/Reception
Enable Transmission/Reception
Erasing
Details of Programming/Erasing
Flash Memory 457
Erasing Data from Flash Memory
(Chip Erase) 461
Notes on Chip Erasing 461
Programming and Erasing Flash Memory
ESCR
Bit Configuration of LIN-UART Extended Status
Control Register (ESCR) 367
Example
Example of Minimum Connection to Flash
Microcomputer Programmer 469
Hardware Connection Example 186
Operating Examples of Timebase Timer 133
Operating Examples of Watch Prescaler 156
Setting Procedure Other than Program
Examples
Setup Procedure Example 134, 145, 157, 171,
246, 275, 291, 322, 432
Execution Time-out Flag
Execution Time-out Flag (DQ5) 455
Explanation
Explanation of Addressing
Explanation of Display Sign of Instruction 482
Explanation of Item in Instruction Table

Extended Communication Control Register
Communication Control Register
(ECCR)
Extended Status Control Register
Bit Configuration of LIN-UART Extended Status
Control Register (ESCR) 367
External Clock
External Clock
External Interrupt
Block Diagram of External Interrupt
Circuit
Block Diagram of Pins Related to External Interrupt
Circuit
Channels of External Interrupt Circuit
External Interrupt Control Register (EIC00) 287
Functions of External Interrupt Circuit
Circuit 289
List of Registers of External Interrupt
Circuit
Operation of External Interrupt Circuit
Pins Related to External Interrupt Circuit
Precautions when Using External Interrupt
Circuit
Registers and Vector Table Related to Interrupts
of External Interrupt Circuit
Sample Programs for External Interrupt
Circuit
External Interrupt Circuit
Block Diagram of External Interrupt
Circuit
Block Diagram of Pins Related to External Interrupt
Circuit
Examples of External Interrupt Circuit
Interrupt During Operation of External Interrupt
Circuit 289
List of Registers of External Interrupt
Circuit
Operation of External Interrupt Circuit
Pins Related to External Interrupt Circuit
Precautions when Using External Interrupt
Circuit
Registers and Vector Table Related to Interrupts
of External Interrupt Circuit
Sample Programs for External Interrupt
Circuit
External Interrupt Control Register
External Interrupt Control Register (EIC00) 287

## F

F <sup>2</sup> MC-8FX	
Instruction Overview of F <sup>2</sup> MC-8FX	481

Feature
Feature of MB95130/M Series2
Features of 256-Kbit Flash Memory
Features of Flash Security
Features of General-purpose Registers
Fixed-cycle Mode
Operation of DWM Timer Function
(Fixed cycle Mode) 217
DWM Timer Eurotion (Fixed avala Mode) 199
F w M Thile Function (Fixed-cycle Mode)
Flag
Data Polling Flag (DQ7)453
Execution Time-out Flag (DQ5)455
Hardware Sequence Flag451
Timing of Reception Interrupt Generation
and Flag Set376
Timing of Transmit Interrupt Generation
and Flag Set378
Toggle Bit 2 Flag (DQ2)456
Toggle Bit Flag (DQ6)454
Flash Memory
Details of Programming/Erasing
Flash Memory
Erasing Data from Flash Memory
(Chin Erase) 461
Features of 256-Khit Flash Memory 444
Flash Memory Programming Procedure 459
Flash Memory Status Register (FSR) 447
Overview of 256 Khit Elash Memory 447
Discing Elash Momery in the Pood/Poset
Flacing Flash Memory in the Read/Reset
Dreemanning and Engine Elect Memory 444
Programming and Erasing Flash Memory
Programming Data into Flash Memory
Register of the Flash Memory
Sector Configuration of 256-Kbit Flash
Memory445
Flash Memory Status Register
Flash Memory Status Register (FSR)447
Flash Microcomputer Programmer
Example of Minimum Connection to Flash
Microcomputer Programmer
Flash Microcontroller
Writing to Elash Microcontroller
Using Parallal Writer 400
Using Faraner writer
Flash Security
Features of Flash Security462
FPT-28P-M17
Package Dimension of FPT-28P-M1710
Free-run Mode
Interval Timer Function (Free-run Mode)188
Operation of Interval Timer Function
(Free-run Mode)
FSR
Flash Momory Status Deviator (ESD) 447
Thash memory status Register (FSR)

Function
A/D Conversion Functions
Bidirectional Communication Function
Block Diagram of Wild Register Function
Function of Reload Counter
Functions of Dedicated Registers
Functions of External Interrupt Circuit
Functions of LIN-UART
Functions of UART/SIO
Input Capture Function
Interrupt when Interval Function is
in Operation130
Interrupts in Operation of Interval Timer Function
(Watch Interrupts)
Interval Timer Function
Interval Timer Function
(Continuous Mode)
Interval Timer Function (Free-run Mode) 188
Interval Timer Function (One-shot Mode) 188
I IN Master/Slave Mode Communication
Europe Europe 207
Master/Slave Mode Communication
Function 404
Operation of Input Capture Function 223
Operation of Interval Timer Function
(Continuous Mode) 213
Operation of Interval Timer Function
(Free run Mode) 215
(Prec-run Mode)
(One shot Mode) 211
(One-shot Mode)
Operation of PWM Timer Function
(Fixed evale Mode) 217
(Fixed-cycle Mode)
(Variable avele Mode) 210
(Valiable-cycle Mode)
Europeian Conversion
Function
Operations of A/D Conversion Function
(Wetch Presseler) 156
(watch Prescaler)
Port 0 Register Function
Port I Register Function
Port F Register Function
Port G Register Function
Pwc Timer Function
PWM Timer Function (Fixed-cycle Mode)
PWM Timer Function
(Variable-cycle Mode)
Watchdog Timer Function
When Interval Timer, Input Capture, or PWC Function
Has Been Selected
Wild Register Function 176

## G

General-purpose Register	
Configuration of General-purpose Registers	37

Features of General-purpose Registers	38
General-purpose Register Area	
(Addresses: $0100_{\rm H}$ to $01FF_{\rm H}$ )	24

#### Н

Handling	
Device Handling Precautions	16
Hardware Connection Example	
Hardware Connection Example	186
Hardware Sequence Flag	
Hardware Sequence Flag	451
Hardware Trigger	
Hardware Trigger	275
How to Write	
How to Write	500

#### I

I/O Circuit	
I/O Circuit Type	13
I/О Мар	
I/O Map	472
I/O Ports	
Overview of I/O Ports	100
ILR	
Configuration of Interrupt Level Setting Register (ILR0 to ILR5)	s 92
Input	
Input Capture Function Input Clock	189 192, 420
Operation of Input Capture Function	223
UART/SIO Serial Input Data Register	
(RDR0)	319
When Interval Timer, Input Capture, or PWC Fund	ction
Has Been Selected	226
Input Capture	
Input Capture Function	189
Operation of Input Capture Function	223
When Interval Timer, Input Capture, or PWC Fund	ction
Has Been Selected	226
Instruction	
Arithmetic Operation Instructions	494
Branch Instructions	495
Explanation of Display Sign of Instruction	482
Explanation of Item in Instruction Table	483
Instruction Map	496
Instruction Overview of F <sup>2</sup> MC-8FX	481
Other Instructions	495
Place at Least Three NOP Instructions Immediate	ely
Following a Standby Mode Setting	
Instruction.	67
Read Destination on the Execution of Bit	
Manipulation Instructions	492
Special Instruction	488

Transfer Instructions	. 493
Instruction Map	
Instruction Map	. 496
Inter-CPU Connection	
Inter-CPU Connection Method	. 389
Interrupt	
An Interrupt Request may Suppress Transition to	
Standby Mode	67
Block Diagram of External Interrupt	07
Circuit	283
Block Diagram of Interrupt Pin Selection	. 200
Circuit	297
Block Diagram of Pins Related to External Intern	unt
Circuit	285
Channels of External Interrupt Circuit	284
Configuration of Interrupt Level Setting Register	s = 0 1
(ILRO to ILR5)	_ 92
External Interrupt Control Register (EIC00)	287
Functions of External Interrupt Circuit	282
Interrupt Acceptance Control Bits	36
Interrupt During Operation of External Interrupt	00
Circuit	289
Interrupt Pin Selection Circuit	205
Interrupt Pin Selection Circuit Control Register	. 200
(WICR)	300
Interrupt Processing	000 93
Interrupt Processing Stack Area	00 90
Interrupt Processing Stack Area	50
Interright Processing Lime	96
Interrupt Processing 1ime	96
Interrupt Processing Time Interrupt Requests from Peripheral Resources	96 90
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is	96 90
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation	96 90 130
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter	96 90 . 130
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation	96 90 . 130 429
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function	96 90 . 130 . 429
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts)	96 90 . 130 . 429 n . 154
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer	96 90 . 130 . 429 n . 154 . 271
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG	96 90 . 130 . 429 n . 154 . 271 . 245
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of UART/SIO	96 90 . 130 . 429 n . 154 . 271 . 245 . 321
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of UART/SIO Interrupts of Watch Counter	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler Interrupts of Watch Prescaler	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154 bit
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt)	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154 bit . 374
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of VART/SIO Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt)	96 90 . 130 . 429 n . 154 . 245 . 321 . 169 . 154 bit . 374
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154 bit . 374
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit	96 90 . 130 . 429 n . 154 . 271 . 154 . 321 . 169 . 154 bit . 374 . 286 95
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of VART/SIO Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit	96 90 . 130 . 429 n . 154 . 271 . 154 . 321 . 169 . 154 bit . 374 . 286 95 . 290
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit	96 90 . 130 . 429 n . 154 . 271 . 154 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Overview of Interrupts	96 90 . 130 . 429 n . 154 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit	96 90 . 130 . 429 n . 154 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90 . 285
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Functio (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit Pins Related to Interrupt Pin Selection	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90 . 285
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit Pins Related to Interrupt Pin Selection Circuit	96 90 . 130 . 429 n . 154 . 271 . 154 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90 . 285 . 298
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit Precautions when Using External Interrupt	96 90 . 130 . 429 n . 154 . 271 . 154 . 245 . 321 . 169 . 154 bit . 374 . 374 . 286 95 . 303 90 . 285 . 298
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation Interrupts in Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit Pins Related to Interrupt Pin Selection Circuit Precautions when Using External Interrupt Circuit	96 90 . 130 . 429 n . 154 . 271 . 154 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90 . 285 . 298
Interrupt Processing Time Interrupt Requests from Peripheral Resources Interrupt when Interval Function is in Operation Interrupts During 8/10-bit A/D Converter Operation of Interval Timer Function (Watch Interrupts) Interrupts of Operation of Interval Timer Function (Watch Interrupts) Interrupts of 16-bit PPG Timer Interrupts of 8/16-bit PPG Interrupts of 8/16-bit PPG Interrupts of Watch Counter Interrupts of Watch Counter Interrupts of Watch Prescaler LIN Synch Field Edge Detection Interrupt (8/16- Compound Timer Interrupt) List of Registers of External Interrupt Circuit Nested Interrupts Operation of External Interrupt Circuit Operation of Interrupt Pin Selection Circuit Pins Related to External Interrupt Circuit Pins Related to Interrupt Pin Selection Circuit Precautions when Using External Interrupt Circuit Reception Interrupt	96 90 . 130 . 429 n . 154 . 271 . 245 . 321 . 169 . 154 bit . 374 . 286 95 . 290 . 303 90 . 285 . 298 . 292 . 372

Register and Vector Table for Interrupts of Timebase
11mer
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts429
Register and Vector Table Related to Interrupts of
Watch Counter169
Register and Vector Table Related to Interrupts of
Watch Prescaler154
Register and Vector Table Related to LIN-UART
Interrupt375
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer271
Registers and Vector Table Related to Interrupts
of 8/16-bit PPG245
Registers and Vector Table Related to Interrupts
of External Interrupt Circuit
Registers and Vector Table Related to UART/SIO
Interrupts
Registers and Vector Tables Related to Interrupts
of 8/16-bit Compound Timer210
Registers Related to Interrupt Pin Selection
Circuit 299
Sample Programs for External Interrupt
Circuit 203
Stack Operation at the Start of Interrupt
Processing 07
Steel Operation upon Datuming
from Interment
Standba Mada is Also Canadad ashar the CDU
Standby Mode is Also Canceled when the CPU
Rejects Interrupts
Table of Interrupt Causes
Timer 00 Interrupt
Timer 01 Interrupt209
Timing of Reception Interrupt Generation
and Flag Set
Timing of Transmit Interrupt Generation
and Flag Set378
Transmission Interrupt321
Transmit Interrupt Request Generation
Timing379
Transmit Interrupts
Interrupt Acceptance Control Bits
Interrupt Acceptance Control Bits
Interrupt Level Setting Registers
Configuration of Interrunt Level Setting Registers
(II R0 to II R5) 92
Interrupt Din Selection Circuit Control Degister
Interrupt Pin Selection Circuit Control Register
(WICK)
Interrupt Requests
Interrupt Requests from Peripheral
Resources90
Interval Function
Interrupt when Interval Function is
in Operation130

Interval Timer
Interrupts in Operation of Interval Timer Function
(Watch Interrupts)154
Interval Timer Function124, 148
Interval Timer Function
(Continuous Mode)188
Interval Timer Function (Free-run Mode)188
Interval Timer Function (One-shot Mode)188
Operation of Interval Timer Function
(Continuous Mode)213
Operation of Interval Timer Function
(Free-run Mode)215
Operation of Interval Timer Function
(One-shot Mode)
<b>Operations of Interval Timer Function</b>
(Watch Prescaler)156
When Interval Timer, Input Capture, or PWC Function
Has Been Selected

## L

LIN	
Asynchronous LIN Mode Operation	98
Bit Configuration of LIN-UART Extended	
Communication Control Register	
(ECCR)	69
Bit Configuration of LIN-UART Extended Status	
Control Register (ESCR)	67
Block Diagram of LIN-UART Pins	57
Functions of LIN-UART3	50
LIN Master Device4	80
LIN Master/Slave Mode Communication	
Function4	07
LIN Slave Device4	09
LIN Synch Field Edge Detection Interrupt (8/16-bit	t
Compound Timer Interrupt)3	74
LIN-UART Baud Rate Selection	80
LIN-UART Bit Configuration of Baud Rate Generat	or
Register (BGR 0/1)3	71
LIN-UART Block Diagram3	53
LIN-UART Pin Direct Access4	01
LIN-UART Pins3	57
LIN-UART Reception Data Register (RDR)3	65
LIN-UART Serial Control Register (SCR)3	59
LIN-UART Serial Mode Register (SMR)3	61
LIN-UART Serial Status Register (SSR)3	63
LIN-UART Transmit Data Register (TDR)3	66
Notes on Using LIN-UART4	10
Operation of LIN-UART3	88
Register and Vector Table Related to LIN-UART	
Interrupt3	75
Register List of LIN-UART3	58
Sample Programs of LIN-UART4	12
LIN-UART	
Bit Configuration of LIN-UART Extended	
Communication Control Register	
(ECCR)	69

Bit Configuration of LIN-UART Extended Status
Control Register (ESCR)
Block Diagram of LIN-UART Pins
Functions of LIN-UART
LIN-UART Baud Rate Selection
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1) 371
LIN-IJART Block Diagram 353
LIN UART Direct Access 401
LIN UADT Ding 257
LIN UART Pagention Data Pagister (DDD) 265
LIN-UART Reception Data Register (RDR)
LIN-UART Serial Control Register (SCR)
LIN-UART Serial Mode Register (SMR)
LIN-UART Serial Status Register (SSR)
LIN-UART Transmit Data Register (TDR) 366
Notes on Using LIN-UART 410
Operation of LIN-UART 388
Register and Vector Table Related to LIN-UART
Interrupt
Register List of LIN-UART 358
Sample Programs of LIN-UART 412
LIN-UART Extended Communication
Bit Configuration of LIN-UART Extended
Communication Control Register
(ECCP) 360
LIN-UART Extended Status Control Register
Bit Configuration of LIN-UART Extended Status
Control Register (ESCR)
LIN-UART Reception Data Register
LIN-UART Reception Data Register (RDR) 365
LIN-UART Serial Control Register
LIN-UART Serial Control Register (SCR)
LIN LIAPT Sorial Mode Projector
LIN UADT Serial Made Desister (SMD) 261
LIN-UAR I Serial Mode Register (SMR)
LIN-UART Serial Status Register
LIN-UART Serial Status Register (SSR)
LIN-UART Transmit Data Register
LIN-UART Transmit Data Register (TDR) 366
List
List of 8/10 bit A/D Converter Registers 423
List of Decisters of External Interrupt
Cirrect
CIFCUIL
Register List of LIN-UART
Low-voltage Detection Reset Circuit
Block Diagram of Low-voltage Detection Reset
Circuit 439
Low-voltage Detection Reset Circuit 438
Operations of Low-voltage Detection Reset
Circuit 441
Pins Related to Low-voltage Detection Reset
Circuit

#### Μ

Main Clock Mode	
Operations in Main Clock Mode	61

Main Stop Mode Operation at the Main Stop Mode
Manipulation
Read Destination on the Execution of Bit
Manipulation Instructions
Mask Option List
Mask Option List 407
Master
Master 400
LIN Master Device
LIN Master/Slave Mode Communication
Function
Master/Slave Mode Communication
Function
Master Device
LIN Master Device 408
MB95130/M Series
Block Diagram of All MB95130/M Series8
Feature of MB95130/M Series2
Pin Assignment of MB95130/M Series9
Product Lineup of MB95130/M Series 4
MDSE
One-shot Mode (MDSE of PCNTH0 Register:
bit 5=1)
PWM Mode (MDSE of PCNTH Register:
bit 5=0)
Memory
Configuration of Memory Space
Details of Programming/Erasing
Flash Memory
Erasing Data from Flash Memory
(Chin Erase)
Features of 256-Kbit Flash Memory
Flash Memory Programming Procedure
Flash Memory Status Register (FSR)
Memory Map
Overview of 256-Kbit Flash Memory
Placement of 16-bit Data in Memory
Placing Flash Memory in the Read/Reset
State
Programming and Erasing Flash Memory
Programming Data into Flash Memory
Register of the Flash Memory
Sector Configuration of 256-Kbit Flash
Memory
Memory Man
Memory Map 23 25 477
Memory Map
Memory Space
Configuration of Memory Space
Minimum Connection
Example of Minimum Connection to Flash
Microcomputer Programmer 469
Mirror Address
Mirror Address for Register Bank and Direct Bank
Pointers

Mode	
8/16-bit Compound Timer 00/01 Timer Mode Contro	ol
Register ch.0 (TMCR0)20	)3
An Interrupt Request may Suppress Transition to	
Standby Mode.	37
Asynchronous LIN Mode Operation	98
Asynchronous Mode Operation	90
Check That Clock-mode Transition	
has been Completed before Setting Standby	y
Mode6	57
Clock Mode State Transition Diagram6	32
Clock Modes	15
Combinations of Clock Mode and Standby	
Mode4	17
Interval Timer Function	
(Continuous Mode)18	38
Interval Timer Function (Free-run Mode)18	38
Interval Timer Function (One-shot Mode)18	38
LIN Master/Slave Mode Communication	
Function40	)7
LIN-UART Serial Mode Register (SMR)	51
Master/Slave Mode Communication	
Function40	)4
One-shot Mode (MDSE of PCNTH0 Register:	
bit 5=1)27	74
Operating Description of UART/SIO Operation	
Mode 0	23
Operating Description of UART/SIO Operation	
Mode 1	30
Operation at the Main Stop Mode17	71
Operation in Sub Stop Mode17	71
Operation of 16-bit PPG Mode25	52
Operation of 8-bit PPG Independent Mode24	17
Operation of 8-bit Prescaler + 8-bit PPG	
Mode24	19
Operation of Interval Timer Function	
(Continuous Mode)21	13
<b>Operation of Interval Timer Function</b>	
(Free-run Mode)21	15
Operation of Interval Timer Function	
(One-shot Mode)21	1
Operation of PWM Timer Function	
(Fixed-cycle Mode)21	17
Operation of PWM Timer Function	
(Variable-cycle Mode)21	9
Operation of Synchronous Mode	
(Operation Mode 2)	94
Operations in Main Clock Mode6	31
Operations in Main PLL Clock Mode6	31
Operations in Sleep Mode7	71
Operations in Standby Mode44	11
Operations in Stop Mode7	72
Operations in Sub PLL Clock Mode	
(on Two-system Clock Product)6	31
Operations in Sub clock Mode	
(on Two-system Clock Product)6	51
Operations in Timebase Timer Mode7	73

Operations in Watch Mode
Oscillation Stabilization Wait Time and Clock Mode/
Overview of Transitions to and from Standby
Mode 66
Peripheral Resources not Affected
by Clock Mode
Pin States in Standby Mode 66
Place at Least Three NOP Instructions Immediately
Following a Standby Mode Setting
Instruction 67
PWM Mode (MDSE of PCNTH Register:
hit 5=0)
PWM Timer Function (Fixed-cycle Mode)
PWM Timer Function
(Variable-cycle Mode)188
Setting 16-bit PPG Mode251
Setting 8-bit Independent Mode
Setting 8-bit Prescaler + 8-bit PPG Mode
Single-chip Mode28
Standby Mode is Also Canceled when the CPU
Rejects Interrupts67
Standby Mode State Transition Diagram68
Standby Modes46
UART/SIO Serial Mode Control Register 1
(SMC10)313
UART/SIO Serial Mode Control Register 2
(SMC20)
Mode Operation
Asynchronous LIN Mode Operation
Asynchronous Mode Operation

#### Ν

Nested Interrupts	
Nested Interrupts	95
Note	
Difference Points among Products and Notes of	n
Selecting a Product	6
Notes on Chip Erasing	461
Notes on Issuing Commands	450
Notes on Use of 8/10-bit A/D Converter	433
Notes on Using LIN-UART	410

## 

One-shot Mode	
Interval Timer Function (One-shot Mode)	.188
One-shot Mode (MDSE of PCNTH0 Register:	
bit 5=1)	.274
<b>Operation of Interval Timer Function</b>	
(One-shot Mode)	.211
Operating	
Operating Description of UART/SIO Operation	
Mode 0	. 323
Operating Description of UART/SIO Operation	
Mode 1	. 330

Operating Examples of Timebase 7	Timer 133
Operating Examples of Watch Pres	scaler 156
Operation	
Arithmetic Operation Instructions.	494
Asynchronous LIN Mode Operatio	n 398
Asynchronous Mode Operation	390
Interrupt During Operation of Exte	rnal Interrupt
Circuit	
Interrupt when Interval Function is	
in Operation	130
Interrupts During 8/10-bit A/D Cor	iverter
Operation	
Interrupts in Operation of Interval	Timer Function
(Watch Interrupts)	
Operating Description of UART/S	O Operation
Mode 0	323
Operating Description of UART/SI	O Operation
Mode 1	.0 operation 330
Operation at the Main Stop Mode	171
Operation in Sub Stop Mode	171
Operation of 16 bit PPG Mode	
Operation of 8 bit PPG Independer	nt Mode 2/7
Operation of 8 bit Prescalar $\pm$ 8 bit	+ DDC
Mode	2/0
Operation of Dedicated Roud Rate	Concretor
(Palaad Counter)	295
(Reload Couller)	
Operation of Input Contume Function	cuit
Operation of Input Capture Function	n
Operation of Interrupt Pin Selection	n Circuit 303
Operation of Interval Timer Function	01
(Continuous Mode)	
Operation of Interval Timer Function	on Ode
(Free-run Mode)	
Operation of Interval Timer Function	on
(Une-shot Mode)	
Operation of LIN-UART	
Operation of PWC Timer Function	
Operation of PWM Timer Function	1
(Fixed-cycle Mode)	
Operation of PWM Timer Function	1
(Variable-cycle Mode)	
Operation of Synchronous Mode	004
(Operation Mode 2)	
Operation of UAR1/SIO	
Operations in Main Clock Mode	
Operations in Main PLL Clock Mo	de 61
Operations in Sleep Mode	
Operations in Standby Mode	
Operations in Stop Mode	
Operations in Sub PLL Clock Mod	e
(on Two-system Clock Pro	oduct) 61
Operations in Sub clock Mode	
(on Two-system Clock Pr	oduct) 61
Operations in Timebase Timer Mo	de 73
Operations in Watch Mode	74
Operations of 8/10-bit A/D Conver	ter's Conversion
Function	430

Operations of A/D Conversion Function
(Watch Prescaler)
Circuit 441
Operations of Port 0
Operations of Port 1 100
Operations of Port F 115
Operations of Port C 120
Operations of Port G
Operations of Prescaler
Operations of Timebase Timer
Operations of Watchdog Timer
Overview of Reset Operation
Read-modify-write Operation
Stack Operation at the Start of Interrupt
Processing
Stack Operation upon Returning
from Interrupt97
Operation Mode
Operating Description of UART/SIO Operation
Mode 0
Operating Description of UART/SIO Operation
Mode 1
Operation of Synchronous Mode
(Operation Mode 2)
Oscillation Stabilization Wait Time
Configuration of Oscillation Stabilization Wait Time
Sotting Degister (WATD) 55
Oscillation Stabilization Wait Time 48
Oscillation Stabilization Wait Time and Clock Mode/
Standby Mode Transition 40
DLL Clash Oppillation Stabilization Weit
Time 40
11me
Oscillation Stabilization Wait Time Setting Register
Configuration of Oscillation Stabilization Wait Time
Setting Register (WATR)55
Other Instructions
Other Instructions 495
Output
8/16-bit PPG Output Inversion Register
(REVC) 244
Output Clock 78 126 150 342
Reset Output 83
UART/SIO Serial Output Data Register
(TDP0) 320
(1DR0)
Instruction Overview of F <sup>2</sup> MC-8FX
Overview of 256-Kbit Flash Memory
Overview of 8/16-bit PPG230
Overview of Clock Controller
Overview of I/O Ports 100
Overview of Interrupts
Overview of Reset Operation
Overview of Transitions to and from Standby
Mode

_
D

Package and Its Corresponding Product Package and Its Corresponding Product7
Package Dimension Package Dimension of FPT-28P-M1710
Parallel Writer
Writing to Flash Microcontroller
Using Parallel Writer499
PC
8/16-bit PPG Timer 00 Control Register ch.0 (PC00)239
8/16-bit PPG Timer 01 Control Register ch.0 (PC01)237
PCNTH
16-bit PPG Status Control Register, Upper Byte (PCNTH0) 267
One-shot Mode (MDSE of PCNTH0 Register:
DWM Mode (MDSE of PCNTH Pagister:
hit 5–0) $272$
16 hit DDC Status Control Degister Lower Pute
(PCNTL0)
PCSRH0, PCSRL0
16-bit PPG Cycle Setting Buffer Registers (PCSRH0, PCSRL0)265
PDCRH0, PDCRL0
16-bit PPG Down Counter Registers
(PDCRH0, PDCRL0)264
PDS
8/16-bit PPG Timer 00/01 Duty Setup Buffer Register (PDS01/PDS00)242
PDUTH0, PDUTL0
16-bit PPG Duty Setting Buffer Registers (PDUTH0, PDUTL0)266
Peripheral Resources
Interrupt Requests from Peripheral Resources 90
Peripheral Resources not Affected
by Clock Mode 45
Pin
Block Diagram of LIN-UART Pins 357
Block Diagram of Pins Related to 8/10-bit A/D
Converter
Block Diagram of Pins Related to 8/16-bit Compound Timer
Block Diagram of Pins Related
to 8/16-bit PPG235
Block Diagram of Pins Related to External Interrupt
Block Diagram of Pins Related
Block Diagrams of Pins Related
to 16-bit PPG262

Operation of Interrupt Pin Selection Circuit303
Pins of 16-bit PPG Timer262
Pins of 8/10-bit A/D Converter
Pins of 8/16-bit PPG234
Pins Related to 8/16-bit Compound Timer
Pins Related to External Interrupt Circuit
Pins Related to Interrupt Pin Selection
Circuit 298
Pins Related to Low-voltage Detection Reset
Circuit 440
Pine Related to UART/SIO 310
Port 0 Pins 102
Port 1 Pins 107
Port F Dins 112
Port C Ding 117
Pin Assignment
Pin Assignment of MB95130/M Series
Pin Connection
Pin Connection18
Pin Description
Pin Description
Pin State
Pin State During a Pasat 84
Din States in Standby Mode
Fin States in Standby Mode
Pin Status
Pin Status in Each Mode479
Place at Least Three NOP Instructions Immediately
Place at Least Three NOP Instructions Immediately
Following a Standby Mode Setting
Following a Standby Mode Setting Instruction
Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately Following a Standby Mode Setting Instruction
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.         Macement         Placement         Placing Flash Memory         Placing Flash Memory         Placing Flash Memory in the Read/Reset         State         State         Operation of PLL Control Register         (PLLC)         Operations in Main PLL Clock Mode         (on Two-system Clock Product)         Mathematical Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PL Clock Mode         (on Two-system Clock Product)         49         PLL Clock Oscillation Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PL Clock Mode
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.         67         Placement         Placement of 16-bit Data in Memory.         99         Placing Flash Memory         Placing Flash Memory         Placing Flash Memory in the Read/Reset         State         State         458         PLL         Configuration of PLL Control Register         (PLLC)         52         Operations in Main PLL Clock Mode         (on Two-system Clock Product)         61         PLL Clock Oscillation Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PLL Clock Mode         0perations in Sub PLL Clock Mode         0perations in Main PLL Clock Mode         0perations in Sub PLL Clock Mode         0perations in Sub PLL Clock Mode
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.         67         Placement         Placement of 16-bit Data in Memory.         99         Placing Flash Memory         Placing Flash Memory in the Read/Reset         State         State         458         PLL         Configuration of PLL Control Register         (PLLC)         52         Operations in Main PLL Clock Mode         (on Two-system Clock Product)         61         PLL Clock Oscillation Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         (on Two system Clock Mode         (on Two system Clock Mode         (operations in Sub PLL Clock Mode
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.         67         Placement         Placement of 16-bit Data in Memory.         99         Placing Flash Memory         Placing Flash Memory in the Read/Reset         State.         458         PLL         Configuration of PLL Control Register         (PLLC).         52         Operations in Main PLL Clock Mode         (on Two-system Clock Product).         61         PLL Clock Oscillation Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PLL Clock Mode         (on Two-system Clock Product).         61         Operations in Main PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Sub PLL Clock Mode         (on Two-system Clock Product).
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.         67         Placement         Placement of 16-bit Data in Memory.         99         Placing Flash Memory         Placing Flash Memory in the Read/Reset         State.         458         PLL         Configuration of PLL Control Register         (PLLC)         52         Operations in Main PLL Clock Mode         (on Two-system Clock Product)         61         PLL Clock Oscillation Stabilization Wait         Time         49         PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Main PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Sub PLL Clock Mode         Operations in Sub PLL Clock Mode         (on Two-system Clock Product)         61         PLL Clock Mode         (on Two-system Clock Product)         61         Operations in Sub PLL Clock Mode         (on Two-
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.       67         Placement       9         Placing Flash Memory       9         Placing Flash Memory       9         Placing Flash Memory       9         PLL       Configuration of PLL Control Register         (PLLC)       52         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         PLL Clock Oscillation Stabilization Wait       1         Time       49         PLL Clock Mode       61         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         PLL Clock Oscillation Stabilization Wait       1         Time       49         PLL Clock Mode       61         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         Operations in Main PLL Clock Mode       61         Operations of PLL Clock Mode       61         Operations of PLL Clock Mode       61         Operation
Place at Least Three NOP Instructions Immediately         Following a Standby Mode Setting         Instruction.       67         Placement       9         Placing Flash Memory       9         Placing Flash Memory in the Read/Reset       39         State       458         PLL       Configuration of PLL Control Register         (PLLC)       52         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         PLL Clock Oscillation Stabilization Wait       1         Time       49         PLL Clock Mode       61         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61         PLL Clock Oscillation Stabilization Wait       1         Time       49         PLL Clock Mode       61         Operations in Main PLL Clock Mode       61         Operations in Sub PLL Clock Mode       61

Port 0	
Block Diagram of Port 0	103
Operations of Port 0	105
Port 0 Configuration	101
Port 0 Pins	102
Port () Register Function	104
Port 1	104
Rlock Diagram of Port 1	108
Operations of Port 1	110
Dort 1 Configuration	107
Point 1 Ding	107
Port 1 Register Function	107
	100
Poil F	440
Block Diagram of Port F	113
Operations of Port F	115
Port F Configuration	112
Port F Pins	112
Port F Register Function	114
Port G	
Block Diagram of Port G	118
Operations of Port G	120
Port G Configuration	117
Port G Pins	117
Port G Register Function	119
PPG	
16-bit PPG Cycle Setting Buffer Registers	
(PCSRH0, PCSRL0)	265
16-bit PPG Down Counter Registers	
(PDCRH0, PDCRL0)	264
16-bit PPG Duty Setting Buffer Registers	
(PDUTH0, PDUTL0)	266
16-bit PPG Status Control Register, Lower Byte	
(PCNTL0)	269
16-bit PPG Status Control Register, Upper Byte	
(PCNTH0)	267
16-bit PPG Timer	258
8/16-bit PPG Output Inversion Register	
(REVC)	244
8/16-bit PPG Start Register (PPGS)	243
8/16-bit PPG Timer 00 Control Register ch 0	2.0
(PC00)	239
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Reg	ister
(PPS01/PPS00)	241
8/16-bit PPG Timer 00/01 Duty Setup Buffer Reg	ister
(PDS01/PDS00)	242
8/16-bit PPG Timer 01 Control Register ch 0	212
(PC01)	237
Block Diagram of 16-bit PPG Timer	259
Block Diagram of 8/16-bit PPG	231
Block Diagram of Pins Related	201
to 8/16 bit PPG	225
Block Diagrams of Pins Palatad	200
to 16 bit DDC	262
Channels of 16 bit DDC Timer	202
Channels of $8/16$ bit DDC	222
Interrupts of 16 bit DDC Timer	200
interrupts of 10-oft FPG filler	211

Interrupts of 8/16-bit PPG 245
Operation of 16 bit DDC Mode 252
Operation of 8 bit DDC Independent Made 247
Operation of 8-bit PPO independent Mode
Operation of 8-bit Prescaler + 8-bit PPG
Mode
Overview of 8/16-bit PPG230
Pins of 16-bit PPG Timer262
Pins of 8/16-bit PPG 234
Precautions when Using 16-bit PPG Timer 276
Precautions when Using 8/16-bit PPG
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer
Registers and Vector Table Related to Interrupts
Pagisters of 16 bit DDC Timor 263
Registers of 10-bit FFG Timer
Registers of 8/10-bit PPG
Sample Programs for 16-bit PPG Timer 277
Sample Programs for 8/16-bit PPG Timer
Setting 16-bit PPG Mode251
Setting 8-bit Prescaler + 8-bit PPG Mode
PPG Timer
16-bit PPG Timer
8/16-bit PPG Timer 00 Control Register ch 0
(PC00) 239
8/16 bit PPC Timer 00/01 Cycle Setup Buffer Pagister
(DDS01/DDS00) 241
(PPS01/PPS00)
8/16-bit PPG Timer 00/01 Duty Setup Butter Register
(PDS01/PDS00)242
8/16-bit PPG Timer 01 Control Register ch.0
(PC01) 237
Block Diagram of 16-bit PPG Timer
Channels of 16-bit PPG Timer
Interrupts of 16-bit PPG Timer 271
Pins of 16-bit PPG Timer
Precautions when Using 16-bit PPG Timer 276
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer
Registers of 16-bit PPG Timer 263
Sample Programs for 16-bit PPG Timer 277
Sample Programs for 2/16 bit DDC Timer 254
Sample Flograms for 8/10-bit FFG Timer
PPGS
8/16-bit PPG Start Register (PPGS)
PPS
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register
(PPS01/PPS00)
Precautions
Device Hendling Presentions 16
Device Handling Flecaulous
Precautions when Using 10-bit PPG Timer
Precautions when Using 8/16-bit Compound
Timer
Precautions when Using 8/16-bit PPG 253
Precautions when Using External Interrupt
recutions when esting External interrupt
Circuit
Circuit
Circuit

Prescaler
Block Diagram of Watch Prescaler
Clearing Watch Prescaler156
Interrupts of Watch Prescaler154
Operating Examples of Watch Prescaler156
Operation of 8-bit Prescaler + 8-bit PPG
Mode249
Operations of Interval Timer Function
(Watch Prescaler)156
Operations of Prescaler
Precautions when Using Watch Prescaler
Prescaler
Prescaler Diock Diagram
Watch Prescaler 154
Register of the Watch Prescaler 151
Sample Programs for Watch Prescaler 159
Setting 8-bit Prescaler + 8-bit PPG Mode 249
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
Watch Prescaler Control Register (WPCR)152
Procedure
Flash Memory Programming Procedure 459
Setting Procedure 389
Setting Procedure Other than Program
Examples
Setup Procedure Example
240, 270, 291, 322, 432
Setup Procedure for Wild Register
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         98
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         185         Interrupt Processing Time
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         10         Processing         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         4         Program
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         4         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer
Setup Procedure for Wild Register
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for 8/26-bit PPG Timer         254         Sample Programs for 8/26-bit PPG Timer
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for External Interrupt         Circuit       293         Sample Programs for UART/SIO       336
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for 16-bit PPG Timer         254         Sample Programs for Watch Counter         293         Sample Programs for UART/SIO         336         Sample Programs for Watch Counter
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         185         Stack Operation at the Start of Interrupt         Processing         186         Stack Operation at the Start of Interrupt         Processing         187         Product Lineup         Product Lineup of MB95130/M Series         187         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for Watch Programs for 16-bit PPG Timer         293         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         170         Processing         Interrupt Processing Stack Area         170         Processing         Interrupt Processing Time         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         170         Product Lineup         Product Lineup of MB95130/M Series         170         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for VART/SIO         336         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         412
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for Watch Counter         293         Sample Programs for Watch Counter         293         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         412         Setting Methods not Covered by Sample
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         434         Setting Methods not Covered by Sample         Programs         Programs
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         434         Setting Methods not Covered by Sample         Programs       434
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         293         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         173         Sample Programs of LIN-UART         434         Setting Methods not Covered by Sample         Programs       434         Setting Procedure Other than Program         Examples       412
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 16-bit PPG Timer         277         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for Watch Counter         173         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         434         Setting Methods not Covered by Sample         Programs       434         Setting Procedure Other than Program         Examples       432
246, 275, 291, 322, 432         Setup Procedure for Wild Register         185         Setup Procedure of Watch Counter         170         Processing         Interrupt Processing Stack Area         93         Interrupt Processing Stack Area         98         Interrupt Processing Time         96         Stack Operation at the Start of Interrupt         Processing         97         Product Lineup         Product Lineup of MB95130/M Series         97         Product Lineup of MB95130/M Series         97         Product Lineup of MB95130/M Series         97         Program         Sample Programs for 8/10-bit A/D         Converter         434         Sample Programs for 8/16-bit PPG Timer         254         Sample Programs for VART/SIO         336         Sample Programs for Watch Counter         173         Sample Programs for Watch Prescaler         159         Sample Programs of LIN-UART         434         Setting Procedure Other than Program         Examples         434         Setu

Programming
Details of Programming/Erasing
Flash Memory457
Flash Memory Programming Procedure459
Programming and Erasing Flash Memory444
Programming Data into Flash Memory459
PSSR
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
PWC
Operation of PWC Timer Function
PWC Timer Function
When Interval Timer, Input Capture, or PWC Function
Has Been Selected
PWM
Operation of PWM Timer Function
(Fixed-cycle Mode)
Operation of PWM Timer Function
(Variable-cycle Mode)219
PWM Mode (MDSE of PCNTH Register:
bit 5=0)272
PWM Timer Function (Fixed-cycle Mode)
PWM Timer Function
(Variable-cycle Mode)188
PWM Timer
Operation of PWM Timer Function
(Fixed-cycle Mode)
Operation of PWM Timer Function
(Variable-cycle Mode)219
PWM Timer Function (Fixed-cycle Mode)
PWM Timer Function
(Variable-cycle Mode)188

## R

RAM	
Effect of Reset on RAM Contents	.84
RDR	
LIN-UART Reception Data Register (RDR)	365
UART/SIO Serial Input Data Register	
(RDR0)	319
Read	
Placing Flash Memory in the Read/Reset	
State	458
Read Destination on the Execution of Bit	
Manipulation Instructions	492
Read-modify-write	
Read-modify-write Operation	492
Reception	
Enable Transmission/Reception	389
LIN-UART Reception Data Register (RDR)	365
Reception Interrupt321,	372
Timing of Reception Interrupt Generation	
and Flag Set	376
Reception Data Register	
LIN-UART Reception Data Register (RDR)	365

Reception Interrupt
Reception Interrupt 321
Timing of Reception Interrupt Generation
and Flag Set
Register
16-bit PPG Cycle Setting Buffer Registers
(PCSRH0, PCSRL0)
16-bit PPG Down Counter Registers
(PDCRH0, PDCRL0)
16-bit PPG Duty Setting Buffer Registers
(PDUTH0, PDUTL0)
16-bit PPG Status Control Register, Lower Byte
(PCNTL0)
16-bit PPG Status Control Register, Upper Byte
(PCNTH0)
8/10-bit A/D Converter Control Register 1
(ADC1)
8/10-bit A/D Converter Control Register 2
(ADC2)
8/10-bit A/D Converter Data Registers Upper/Lower
(ADDH,ADDL)
8/16-bit Compound Timer 00/01 Control Status
Register 0 (T00CR0/T01CR0) 197
8/16-bit Compound Timer 00/01 Control Status
Register 1 (T00CR1/T01CR1) 200
8/16-bit Compound Timer 00/01 Data Register
(T00DR/T01DR)
8/16-bit Compound Timer 00/01 Timer Mode Control
Register ch.0 (TMCR0) 203
8/16-bit PPG Output Inversion Register
(REVC)
8/16-bit PPG Start Register (PPGS)
8/16-bit PPG Timer 00 Control Register ch.0
(PC00)
8/16-bit PPG 11mer 00/01 Cycle Setup Buffer Register
(PPS01/PPS00)
8/10-011 PPG TIMET 00/01 Duty Setup Dutter Register
(PDS01/PDS00)
$\frac{8}{10-011}$ (DC01) Control Register cn.0
(FC01)
Communication Control Register
(ECCR) 369
Bit Configuration of LIN-UART Extended Status
Control Register (ESCR) 367
Block Diagram of Wild Register Function 177
Configuration of Condition Code Register
(CCR)
Configuration of Dedicated Registers
Configuration of General-purpose Registers
Configuration of Interrupt Level Setting Registers
(ILR0 to ILR5)
Configuration of Oscillation Stabilization Wait Time
Setting Register (WATR) 55
Configuration of PLL Control Register
(PLLC)
Configuration of Register Bank Pointer (RP) 32

Configuration of Reset Source Register
(RSRR)
Configuration of System Clock Control Register
(SYCC)
External Interrupt Control Register (EIC00) 287
Features of General-purpose Registers
Flash Memory Status Register (FSR) 447
Functions of Dedicated Registers
General-purpose Register Area
(Addresses: $0100_{\rm H}$ to $01FF_{\rm H}$ )
Interrupt Pin Selection Circuit Control Register
(WICR)
LIN-UART Bit Configuration of Baud Rate Generator
Register (BGR 0/1) 371
LIN-UART Reception Data Register (RDR) 365
LIN-UART Serial Control Register (SCR)
LIN-UART Serial Mode Register (SMR)
LIN-UART Serial Status Register (SSR)
LIN-UART Transmit Data Register (TDR)
List of 8/10-bit A/D Converter Registers 423
List of Registers of External Interrupt
Circuit
Mirror Address for Register Bank and Direct Bank
Pointers
One-shot Mode (MDSE of PCNTH0 Register:
bit 5=1)
Port 0 Register Function 104
Port 1 Register Function 109
Port F Register Function 114
Port G Register Function 119
PWM Mode (MDSE of PCNTH Register:
bit 5=0)
Register and Vector Table for Interrupts of Timebase
Timer
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts
Register and Vector Table Related to Interrupts of
Watch Counter
Register and Vector Table Related to Interrupts of
Watch Prescaler
Register and Vector Table Related to LIN-UART
Interrupt
Register List of LIN-UART
Register of the Flash Memory 446
Register of the Timebase Timer 127
Register of the Watch Prescaler 151
Register of the Watchdog Timer 141
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer 271
Registers and Vector Table Related to Interrupts
of 8/16-bit PPG 2/15
Registers and Vector Table Related to Interrupts
of External Interrupt Circuit 220
Registers and Vector Table Related to UAPT/SIO
Interrunts 221
шениро

Registers and Vector Tables Related to Interrupts
of 8/16-bit Compound Timer210
Registers of 16-bit PPG Timer263
Registers of 8/16-bit PPG236
Registers of Watch Counter165
Registers Related to 8/16-bit Compound
1 imer
Registers Related to Interrupt Pin Selection
Registers Related to UAR1/SIU
Registers Related to UAR1/SIO Dedicated Baud Rate Generator 344
Registers Related to Wild Register 179
Setup Procedure for Wild Register 185
Standby Control Register (STBC) 58
Timebase Timer Control Register (TBTC) 128
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR)
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
UART/SIO Serial Input Data Register
(RDR0)
UART/SIO Serial Mode Control Register 1
(SMC10)
UART/SIO Serial Mode Control Register 2
(SMC20)
UART/SIO Serial Output Data Register
(TDR0)
UART/SIO Serial Status and Data Register
(SSR0)
Watch Counter Control Register (WCSR)
Watch Counter Data Register (WCDR)
Watch Prescaler Control Register (WPCR)
Watchdog Timer Control Register (WDTC)
Wild Register Address Compare Enable Register
(WREN) 18:
Wild Register Address Setup Registers
(WRAR0 to WRAR2) 182
Wild Register Applicable Addresses 185
Wild Register Data Setup Registers
(WRDR0 to WRDR2) 181
Wild Register Data Test Setup Register
(WROR) 184
Wild Register Function 176
Wild Register Number 180
Pogistor Bank
Configuration of Pagistar Bank Dointor (DD) 3'
Mirror Address for Pagister Bank and Direct Bank
Militor Address for Register Dank and Direct Dank
Folliters
Keload Counter
Function of Reload Counter
Operation of Dedicated Baud Rate Generator
(Reload Counter)
Reload Value
Reload Value and Baud Rate
of Each Clock Speed

Reset
Block Diagram of Low-voltage Detection Reset
Circuit
Configuration of Reset Source Register
(RSRR)
Effect of Reset on RAM Contents
Low-voltage Detection Reset Circuit
Operations of Low-voltage Detection Reset
Circuit
Overview of Reset Operation
Pin State During a Reset
Pins Related to Low-voltage Detection Reset
Circuit
Placing Flash Memory in the Read/Reset
State
Reset Factors
Reset Output
Reset Time
Reset Operation
Overview of Reset Operation
Reset Source Register
Configuration of Reset Source Register
(RSRR) 86
Roult
Dita Desult Information Dita 25
Bits Result Information Bits
Returning
Stack Operation upon Returning
from Interrupt
REVC
8/16-bit PPG Output Inversion Register
(REVC)244
RP
Configuration of Register Bank Pointer (RP)32
RSRR
Configuration of Reset Source Register
(RSRR)

## S

Sample
Sample Programs for 16-bit PPG Timer277
Sample Programs for 8/10-bit A/D
Converter
Sample Programs for 8/16-bit PPG Timer254
Sample Programs for External Interrupt
Circuit
Sample Programs for UART/SIO
Sample Programs for Watch Counter
Sample Programs for Watch Prescaler
Sample Programs of LIN-UART412
Setting Methods not Covered by Sample
Programs
Setup Methods without Sample
Program159, 254, 277, 293, 336
Programs

Sample Program
Setup Methods without Sample
Program 254, 277, 293, 336
SCR
LIN-UART Serial Control Register (SCR)
Sector Configuration
Sector Configuration
Sector Configuration of 256-Kbit Flash
Memory
Selecting
Difference Points among Products and Notes on
Selecting a Product 6
Selection
Plack Diagram of Interrupt Din Selection
Circuit 207
Interrupt Din Selection Circuit 200
Interrupt Fin Selection Circuit Control Pagister
(WICD) 200
(WICK)
Operation of Interrupt Din Selection Circuit 202
Ding Deleted to Interrupt Pin Selection
Circuit 200
Desistors Delated to Interrupt Din Selection
Circuit 200
LIADT/SIO Dedicated David Data Concenter Dresseler
Selection Decister (DSSD) 245
Selection Register (PSSR)
Serial Control Register
LIN-UART Serial Control Register (SCR)
Serial Input Data Register
UART/SIO Serial Input Data Register
(RDR0)
Serial Mode Control Register
UART/SIO Serial Mode Control Register 1
(SMC10)
UART/SIO Serial Mode Control Register 2
(SMC20)
Serial Mode Register
LIN-UART Serial Mode Register (SMR)
Serial Output Data Register
UART/SIO Serial Output Data Register
(TDR0) 320
Sarial Status and Data Pagistar
JUADT/SIO Serial Status and Data Desister
UAR I/SIO Serial Status and Data Register
(SSKU)
Serial Status Register
LIN-UART Serial Status Register (SSR)
Setting
16-bit PPG Cycle Setting Buffer Registers
(PCSRH0, PCSRL0)
16-bit PPG Duty Setting Buffer Registers
(PDUTH0, PDUTL0)
Baud Rate Setting
Check That Clock-mode Transition
has been Completed before Setting Standby
Mode

Configuration of Interrupt Level Setting Registers
Configuration of Oscillation Stabilization Wait Time
Setting Register (WATR)
Place at Least Three NOP Instructions Immediately
Following a Standby Mode Setting
Instruction
Setting 16-bit PPG Mode251
Setting 8-bit Independent Mode247
Setting 8-bit Prescaler + 8-bit PPG Mode
Setting Methods not Covered by Sample
Programs
Setting Procedure
Setting Procedure Other than Program
Examples 412
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR)
Setting Procedure
Setting Procedure
Setting Procedure Other than Program
Examples 412
Setup
8/16-bit PPG Timer 00/01 Cycle Setup Buffer Register
(PPS01/PPS00)
8/16-bit PPG Timer 00/01 Duty Setup Buffer Register
(PDS01/PDS00)242
Setup Methods without Programs
Setup Methods without Sample
Program
Setup Procedure Example 134, 145, 157, 171,
240, 275, 291, 522, 452 Sotup Procedure for Wild Pagister 185
Setup Procedure of Watch Counter 170
Wild Register Address Setup Registers
(WRAR0 to WRAR2) 182
Wild Register Data Setun Registers
(WRDR0 to WRDR2)
Wild Register Data Test Setup Register
(WROR)
Signaling
Signaling 389
Single-chip Mode
Single-chip Mode 28
Block Diagram of Ding Balatad
to UAPT/SIO 311
Block Diagram of UART/SIO 307
Block Diagram of UART/SIO Dedicated Baud Rate
Generator 342
Channels of UART/SIO
Channels of UART/SIO Dedicated Baud Rate
Generator
Functions of UART/SIO
Interrupts of UART/SIO
Operating Description of UART/SIO Operation
Mode 0 323

Operating Description of UART/SIO Operation
Mode 1
Operation of UART/SIO322
Pins Related to UART/SIO310
Registers and Vector Table Related to UART/SIO
Interrupts
Registers Related to UART/SIO
Registers Related to UART/SIO Dedicated Baud Rate
Generator
Sample Programs for UART/SIO
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR)346
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
UART/SIO Serial Input Data Register
(RDR0)
UART/SIO Serial Mode Control Register 1
(SMC10)313
UART/SIO Serial Mode Control Register 2
(SMC20)
UART/SIO Serial Output Data Register
(TDR0)
UART/SIO Serial Status and Data Register
(SSR0)
Slave
LIN Master/Slave Mode Communication
Function 407
LIN Slave Device 400
Master/Slave Mode Communication
Function 404
Slave Device
LIN Slave Device409
Sleep
Operations in Sleep Mode71
Sleep Mode
Operations in Sleep Mode71
SMC
UART/SIO Serial Mode Control Register 1
(SMC10) 313
UART/SIO Serial Mode Control Register 2
(SMC20) 315
(SMC20)
SMR
LIN-UART Serial Mode Register (SMR)
Source
Configuration of Reset Source Register
(RSRR)86
Special Instruction
Special Instruction
SSR
LIN-UART Serial Status Register (SSR) 363
UART/SIO Serial Status and Data Register
(SSR0) 317
Stack
Interment Drogosoin - Steal Area
Interrupt Processing Stack Area

Stack Operation at the Start of Interrupt
Processing97
Stack Operation upon Returning
from Interrupt97
Stack Area
Interrupt Processing Stack Area98
Stack Operation
Stack Operation at the Start of Interrupt
Processing
Stack Operation upon Returning
from Interrupt
Standby
An Interrupt Request may Suppress Transition to
Standby Mode 67
Check That Clock-mode Transition
has been Completed before Setting Standby
Mode 67
Combinations of Clock Mode and Standby
Mode 47
Mode
Operations III Standby Mode
Standbar Mada Transition
Standby Mode Transition
Overview of Transitions to and from Standby
Mode
Pin States in Standby Mode
Place at Least Three NOP Instructions Immediately
Following a Standby Mode Setting
Instruction
Standby Control Register (STBC)58
Standby Mode is Also Canceled when the CPU
Rejects Interrupts67
Standby Mode State Transition Diagram68
Standby Modes46
Standby Control Register
Standby Control Register (STBC)58
Standby Mode
An Interrupt Request may Suppress Transition to
Standby Mode 67
Check That Clock-mode Transition
has been Completed before Setting Standby
Mode 67
Combinations of Clock Mode and Standby
Mode 47
Operations in Standby Mode 111
Operations in Standby Mode
Standby Mode Transition 40
Overview of Transitions to and from Standby
Mode 66
Mode
Plin States in Standby Wode
Frace at Least 1 nree NOP instructions immediately
Following a Standby Mode Setting
Instruction
Standby Mode is Also Canceled when the CPU
Rejects Interrupts
Standby Mode State Transition Diagram68
Standby Modes46

Start
8/16-bit PPG Start Register (PPGS)
Processing97
State
Clock Mode State Transition Diagram
Placing Flash Memory in the Read/Reset
State
Standby Mode State Transition Diagram
16-bit PPG Status Control Register, Lower Byte (PCNTL0) 269
16-bit PPG Status Control Register, Upper Byte
8/16-bit Compound Timer 00/01 Control Status
Register 0 (T00CR0/T01CR0) 197 8/16-bit Compound Timer 00/01 Control Status
Register 1 (T00CR1/T01CR1) 200 Bit Configuration of LIN-UART Extended Status
Control Register (ESCR)
Flash Memory Status Register (FSR) 447
LIN-UART Serial Status Register (SSR)
UART/SIO Serial Status and Data Register (SSR0)
Status Register
8/16-bit Compound Timer 00/01 Control Status Register 1 (T00CR1/T01CR1)
STBC
Standby Control Register (STBC)
Stop
Operation at the Main Stop Mode 171
Operation in Sub Stop Mode 171
Operations in Stop Mode72
Stop Mode
Operation at the Main Stop Mode 171
Operation in Sub Stop Mode 171
Operations in Stop Mode72
Sub Stop Mode
Operation in Sub Stop Mode 171
Sub Clock Mode
Operations in Sub Clock Mode
(on Two-system Clock Product)
SYCC
Configuration of System Clock Control Register
(SYCC)
Synchronous Method
Synchronous Method
Synchronous Mode
Operation of Synchronous Mode
(Operation Mode 2) 394
System
Configuration of System Clock Control Register (SYCC)

System Clock Control Register
Configuration of System Clock Control Register
(SYCC)
т
T00CR0/T01CR0
8/16-bit Compound Timer 00/01 Control Status
Register 0 (T00CR0/T01CR0) 197

Register 0 (100CR0/101CR0) 197
T00CR1/T01CR1
8/16-bit Compound Timer 00/01 Control Status
Register 1 (T00CR1/T01CR1) 200
8/16-bit Compound Timer 00/01 Data Register
(100DR/101DR)
Table
Command Sequence Table 449
Explanation of Item in Instruction Table
Register and Vector Table for Interrupts of Timebase
Timer
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts 429
Register and Vector Table Related to Interrupts of
Wetch Counter 160
Pagister and Vester Table Delated to Interments of
Register and vector rable Related to Interrupts of
Watch Prescaler
Register and Vector Table Related to LIN-UART
Interrupt
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer 271
Registers and Vector Table Related to Interrupts
of 8/16-bit PPG245
Registers and Vector Table Related to Interrupts
of External Interrupt Circuit
Registers and Vector Table Related to UART/SIO
Interrupts
Table of Interrupt Causes 476
Vector Table Area
(A ddresses; EEC0 to EEEE) 24
(Addresses: ITCO <sub>H</sub> to ITTT <sub>H</sub> )24
TBTC
Timebase Timer Control Register (TBTC) 128
TDR
LIN-UART Transmit Data Register (TDR)
UART/SIO Serial Output Data Register
(TDR0)
Timohaca Timor
Diask Diagram of Timehees Timer 125
Charlies Time Time as Time 123
Clearing Timebase Timer
Operating Examples of Timebase Timer
Operations of Timebase Timer 132
Precautions when Using Timebase Timer
Register and Vector Table for Interrupts of Timebase
Timer 131
Register of the Timebase Timer 127
Timebase Timer Control Register
· · · · · · · · · · · · · · · · · · ·

Timebase Timer Control Register (TBTC) 12
---

Timebase Timer Mode
Timer 00
Timer 00 Interrupt
Timer 01
Timer 01 Interrupt209
Timing
and Flag Set
Timing of Transmit Interrupt Generation
and Flag Set378
Transmit Interrupt Request Generation
TIMMIg
8/16-bit Compound Timer 00/01 Timer Mode Control
Register ch.0 (TMCR0)203
Toggle Bit 2 Flag
Toggle Bit 2 Flag (DQ2)456
Toggle Bit Flag
Toggle Bit Flag (DQ0)434
Transfer Instructions
Transfer Instructions
Transfer Instructions493
Transition
An Interrupt Request may Suppress Transition to
Check That Clock-mode Transition
has been Completed before Setting Standby
Mode67
Clock Mode State Transition Diagram
Standby Mode Transition 49
Overview of Transitions to and from Standby
Mode66
Standby Mode State Transition Diagram68
Transmission
Transmission Interrupt 321
Transmission Interrupt
Transmission Interrupt
Transmit
Timing of Transmit Interrupt Generation
and Flag Set
Transmit Interment Dequest Constration
Transmit Interrupt Request Generation Timing

#### U

UART	
Bit Configuration of LIN-UART Extended	
Communication Control Register	
(ECCR)	. 369
Bit Configuration of LIN-UART Extended Status	5
Control Register (ESCR)	.367
Block Diagram of LIN-UART Pins	.357
Block Diagram of Pins Related	
to UART/SIO	.311
Block Diagram of UART/SIO	. 307
Block Diagram of UART/SIO Dedicated Baud R	ate
Generator	. 342
Channels of UART/SIO	. 309
Channels of UART/SIO Dedicated Baud Rate	
Generator	. 343
Functions of LIN-UART	. 350
Functions of UART/SIO	. 306
Interrupts of UART/SIO	.321
LIN-UART Baud Rate Selection	.380
LIN-UART Bit Configuration of Baud Rate Gener	rator
Register (BGR 0/1)	.371
LIN-UART Block Diagram	.353
LIN-UART Pin Direct Access	.401
LIN-UART Pins	. 357
LIN-UART Reception Data Register (RDR)	. 365
LIN-UART Serial Control Register (SCR)	.359
LIN-UART Serial Mode Register (SMR)	.361
LIN-UART Serial Status Register (SSR)	.363
LIN-UART Transmit Data Register (TDR)	.366
Notes on Using LIN-UART	.410
Operating Description of UART/SIO Operation	~~~
	. 323
Operating Description of UAR1/SIO Operation	220
Mode 1	. 330 200
Operation of LAPT/SIO	. 300 222
Ding Delated to UART/SIO	. 322 310
Pagister and Vactor Table Polated to LIN UAPT	.310
Interrupt	375
Register List of LIN-IJART	358
Registers and Vector Table Related to UART/SI	. ວວວ ົ
Interrupts	
Registers Related to UART/SIO	312
Registers Related to UART/SIO Dedicated Baud	Rate
Generator	.344
Sample Programs for UART/SIO	.336
Sample Programs of LIN-UART	.412
UART/SIO Dedicated Baud Rate Generator Bau	d
Rate Setting Register (BRSR)	.346
UART/SIO Dedicated Baud Rate Generator Press	caler
Selection Register (PSSR)	.345
UART/SIO Serial Input Data Register	
(RDR0)	. 319

UART/SIO Serial Mode Control Register 1
UART/SIO Serial Mode Control Register 2
(SMC20)
UART/SIO Serial Output Data Register
(IDR0)
(SSR0)
LIART/SIO
Block Diagram of Pins Related
to UART/SIO 311
Block Diagram of UART/SIO 307
Block Diagram of UART/SIO Dedicated Baud Rate
Generator 342
Channels of UART/SIO 309
Channels of UART/SIO Dedicated Baud Rate
Generator 343
Functions of UART/SIO 306
Interrupts of UART/SIO 321
Operating Description of UART/SIO Operation
Mode 0 323
Operating Description of UAPT/SIO Operation
Mode 1 330
Mode 1
Ding Deleted to UADT/SIO 210
Phils Related to UART/SIO
Registers and vector rable Related to UART/SIO
Desisters Deleted to UADT/CIO 212
Registers Related to UAR 1/SIO
Registers Related to UAR I/SIO Dedicated Baud Rate
Generator
Sample Programs for UART/SIO
UAR I/SIU Dedicated Baud Rate Generator Baud
Kate Setting Register (BRSR)
UAR I/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
UARI/SIO Serial Input Data Register
(RDR0)
UART/SIO Serial Mode Control Register 1
(SMC10)
UAR I/SIO Serial Mode Control Register 2
(SMC20)
UAR I/SIO Serial Output Data Register
(1DR0)
UART/SIO Serial Status and Data Register
(SSR0)
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register
UART/SIO Dedicated Baud Rate Generator Baud
Rate Setting Register (BRSR) 346
UART/SIO Dedicated Baud Rate Generator
Prescaler Selection Register
UART/SIO Dedicated Baud Rate Generator Prescaler
Selection Register (PSSR)
UART/SIO Serial Input Data Register
UART/SIO Serial Input Data Register
(RDR0)

UART/SIO Serial Mode Control Register	
(SMC10)	313
UART/SIO Serial Mode Control Register 2	
(SMC20)	315
UART/SIO Serial Output Data Register	
UART/SIO Serial Output Data Register	
(TDR0)	320
UART/SIO Serial Status and Data Register	
UART/SIO Serial Status and Data Register	
(SSR0)	317

#### 

Variable-cycle Mode
Operation of PWM Timer Function
(Variable-cycle Mode)
PWM Timer Function
(Variable-cycle Mode)188
Vector
Registers and Vector Table Related to UART/SIO
Interrupts
Vector Table
Register and Vector Table for Interrupts of Timebase
Timer131
Register and Vector Table Related to 8/10-bit A/D
Converter Interrupts 429
Register and Vector Table Related to Interrupts of
Watch Counter169
Register and Vector Table Related to Interrupts of
Watch Prescaler 154
Register and Vector Table Related to LIN-UART
Interrupt
Registers and Vector Table Related to Interrupts
of 16-bit PPG Timer
Registers and vector Table Related to Interrupts
01 8/10-Dil PPG
of External Interrupt Circuit 280
Di Externar Interrupt Circuit
Interrupts 321
Registers and Vector Tables Related to Interrupts
of 8/16-bit Compound Timer 210
Vector Table Area
(Addresses: $FFCO_{11}$ to $FFFF_{11}$ ) 24

## W

Watch Counter	
Block Diagram of Watch Counter	163
Interrupts of Watch Counter	169
Register and Vector Table Related to Interru	upts of
Watch Counter	169
Registers of Watch Counter	165
Sample Programs for Watch Counter	173
Setup Procedure of Watch Counter	170
Watch Counter	162

Watch Counter Control Register (WCSR)167 Watch Counter Data Register (WCDR)166
Watch Counter Control Register Watch Counter Control Register (WCSR)
Watch Counter Data Register
Watch Counter Data Register (WCDR)166
Watch Interrupts
Interrupts in Operation of Interval Timer Function
(Watch Interrupts)154
Watch Mode
Operations in Watch Mode 74
Wateh Dragoglar
Plack Diagram of Wotch Proceeder 140
Clearing Wetch Decesler
Listerments of Wetch Dresseler
Interrupts of watch Prescaler
Operating Examples of Watch Prescaler
Operations of Interval Timer Function
(Watch Prescaler)
Precautions when Using Watch Prescaler158
Register and Vector Table Related to Interrupts of
Watch Prescaler154
Register of the Watch Prescaler151
Sample Programs for Watch Prescaler159
Watch Prescaler Control Register (WPCR)152
Watch Prescaler Control Register
Watch Prescaler Control Register (WPCR)152
Watchdog Timer
Block Diagram of Watchdog Timer
Operations of Watchdog Timer
Precautions when Using Watchdog Timer
Register of The Watchdog Timer
Watchdog Timer Control Register (WDTC)142
Watchdog Timer Function 138
Watchdog Timer Control Pagistor
Watchdog Timer Control Register (WDTC) 1/2
Webb Account of the Desister (WODD)
watch Counter Data Register (WCDR)100
WCSR
Watch Counter Control Register (WCSR)167
WDTC
Watchdog Timer Control Register (WDTC)142
WICR
Interrupt Pin Selection Circuit Control Register
(WICR)
Wild Register
Block Diagram of Wild Register Function 177
Registers Related to Wild Register 179
Setup Procedure for Wild Register 185
Wild Register Address Compare Enable Register
(WREN) 183
Wild Register Address Setun Registers
(WRAR0 to WRAR2)  182
Wild Register Applicable Addresses 185
Wild Register Data Setup Registers
(WRDR0 to WRDR2)181
· · · · · · · · · · · · · · · · · · ·

Wild Register Data Test Setup Register
(WROR)184
Wild Register Function176
Wild Register Number 180
Wild Register Address Compare Enable Register Wild Register Address Compare Enable Register
(WREN)
Wild Register Address Setup Registers Wild Register Address Setup Registers (WRAR0 to WRAR2)182
Wild Register Data Setup Registers Wild Register Data Setup Registers (WRDR0 to WRDR2)181
Wild Register Data Test Setup Register Wild Register Data Test Setup Register (WROR)
WPCR
Watch Prescaler Control Register (WPCR) 152

WRAR Wild Register Address Setup Registers (WRAR0 to WRAR2)182
WRDR
Wild Register Data Setup Registers
(WRDR0 to WRDR2) 181
WREN
Wild Register Address Compare Enable Register (WREN)
Write
How to Write
Writing
Writing to Flash Microcontroller
Using Parallel Writer 499
WROR
Wild Register Data Test Setup Register (WROR)184
Input level selection register......100 Input level selection register2......100

# **Register Index**

#### Α

A/D control register 1	424
A/D control register 2	426
A/D data register upper	428
A/D data register lower	428
A/D input disable register lower	100
	A/D control register 1 A/D control register 2 A/D data register upper A/D data register lower A/D input disable register lower

# В

BGR0	LIN-UART baud rate generator register 0
BGR1	LIN-UART baud rate generator register 1
BRSR0	UART/SIO dedicated baud rate generator
	baud rate setting register ch0 346

#### D

DDR0	Port 0 direction register 100
DDR1	Port 1 direction register 100
DDRF	Port F direction register 100
DDRG	Port G direction register100

#### Е

ECCR	LIN-UART extended communication control register
EIC00	External interrupt control register ch0/1
EIC10	External interrupt control register ch2/3
EIC20	External interrupt control register ch4/5
EIC30	External interrupt control register ch6/7
ESCR	LIN-UART extended status control register 367

# F

FSR	Flash memory status register 447
I	
ILR0	Interrupt level setting register 0 92
ILR1	Interrupt level setting register 1
ILR2	Interrupt level setting register 2 92
ILR3	Interrupt level setting register 3 92
ILR4	Interrupt level setting register 4 92
ILR5	Interrupt level setting register 5

Р	
PC00	8/16-bit PPG timer 00 control register ch0 239
PC01	8/16-bit PPG timer 01 control register ch0 237
PC10	8/16-bit PPG timer 00 control register ch1 239
PC11	8/16-bit PPG timer 01 control register ch1 237
PCNTH0	16-bit PPG status control register upper ch0 267
PCNTL0	16-bit PPG status control register lower ch0
PCSRH0	16-bit PPG cycle setting buffer register upper ch0265
PCSRL0	16-bit PPG cycle setting buffer register lower ch0265
PDCRH0	16-bit PPG down counter register upper ch0
PDCRL0	16-bit PPG down counter register lower ch0
PDR0	Port 0 data register100
PDR1	Port 1 data register100
PDRF	Port F data register100
PDRG	Port G data register100
PDS00	8/16-bit PPG timer 00 duty setting buffer register ch0242
PDS01	8/16-bit PPG timer 01 duty setting buffer register ch0242
PDS10	8/16-bit PPG timer 00 duty setting buffer register ch1242
PDS11	8/16-bit PPG timer 01 duty setting buffer register ch1242
PDUTH0	16-bit PPG duty setting buffer register upper ch0266
PDUTL0	16-bit PPG duty setting buffer register lower ch0266
PLLC	PLL control register
PPGS	8/16-bit PPG start register
PPS00	8/16-bit PPG timer 00 cvcle setup buffer
	register ch0
PPS01	8/16-bit PPG timer 01 cycle setup buffer
	register ch0241

ILSR

ILSR2

### **Register Index**

PPS10	8/16-bit PPG timer 00 cycle setup buffer
	register ch1241
PPS11	8/16-bit PPG timer 01 cycle setup buffer
	register ch1241
PSSR0	UART/SIO dedicated baud rate generator
	prescaler selection register ch0345
PUL0	Port 0 pull-up register100
PUL1	Port 1 pull-up register100
PULG	Port G pull-up register100

# R

RDR/TDI	RLIN-UART reception /transmit data regis	ter 65
RDR0	UART/SIO serial input data register ch0	40
REVC	8/16-bit PPG output inversion register	19
	2	.44
RSSR	Reset source register	86

## S

SCR	LIN-UART serial control register	359
SMC10	UART/SIO serial mode control register	1
	ch0	313
SMC20	UART/SIO serial mode control register	2
	ch0	315
SMR	LIN-UART serial mode register	361
SSR	LIN-UART serial status register	363
SSR0	UART/SIO serial status and data registed	er
	ch0	317
STBC	Standby control register	58
SYCC	System clock control register	50

# Т

T00CR0	8/16-bit composite timer 00 control status	
	register 0 ch019	<b>}</b> 7
T00CR1	8/16-bit composite timer 00 control status	
	register 1 ch020	)0
T00DR	8/16-bit composite timer 00 data register	
	ch020	)6
T01CR0	8/16-bit composite timer 01 control status	
	register 0 ch019	97

T01CR1	8/16-bit composite timer 01 control status
	register 1 ch0 200
T01DR	8/16-bit composite timer 01 data register
	ch0206
TBTC	Timebase timer control register 128
TDR0	UART/SIO serial output data register ch0
TMCR0	8/16-bit composite timer 00/01 timer mode
	control register ch0 203

#### w

WATR	Oscillation stabilization wait time setting	5
WCDR	Watch counter data register	6
WCSR	Watch counter control register	7
WDTC	Watchdog timer control register	2
WICR	Interrupt pin selection circuit control registe	r 9
WPCR	Watch prescaler control register 152	2
WRARH	OWild register address setup register upper ch018	2
WRARH	1Wild register address setup register upper ch118	2
WRARH	2Wild register address setup register upper ch218	2
WRARLO	Wild register address setup register lower ch018	2
WRARL1	Wild register address setup register lower ch118	2
WRARL2	2 Wild register address setup register lower ch218	2
WRDR0	Wild register data setup register ch0	1
WRDR1	Wild register data setup register ch1	1
WRDR2	Wild register data setup register ch2	1
WREN	Wild register address compare enable register	3
WROR	Wild register data test setup register	4

# **Pin Function Index**

#### Α

ADTG	A/D converter trigger input pin 42	1
AN00	A/D converter analog input pin ch0 42	1
AN01	A/D converter analog input pin ch1 42	1
AN02	A/D converter analog input pin ch2 42	1
AN03	A/D converter analog input pin ch3 42	1
AN04	A/D converter analog input pin ch4 42	1
AN05	A/D converter analog input pin ch5 42	1
AN06	A/D converter analog input pin ch6 42	1
AN07	A/D converter analog input pin ch7 42	1
AV <sub>CC</sub>	A/D converter power supply pin 42	1
AV <sub>SS</sub>	A/D converter ground pin 42	1
E		

#### I

INT00	External interrupt input pin ch0
INT01	External interrupt input pin ch1 285
INT02	External interrupt input pin ch2 285
INT03	External interrupt input pin ch3 285
INT04	External interrupt input pin ch4285
INT05	External interrupt input pin ch5285
INT06	External interrupt input pin ch6285
INT07	External interrupt input pin ch7 285
IVI	
MOD	Mode pin

#### Ρ

PPG0	16-bit PPG output pin ch0	262
PPG00	8/16-bit PPG timer 00 output pin ch0	234
PPG01	8/16-bit PPG timer 01 output pin ch0	
PPG10	8/16-bit PPG timer 00 output pin ch1	234
		235
PPG11	8/16-bit PPG timer 01 output pin ch1	225
		200

#### S

SCK	LIN-UART clock input/output pin	.357
SIN	LIN-UART serial data input pin	.357
SOT	LIN-UART serial data output pin	.357

#### Т

TO00	8/16-bit composite timer 00 output pin ch0
TO01	8/16-bit composite timer 01 output pin ch0
	194
TRG0	16-bit PPG trigger input pin ch0262

#### U

UCK0	0 UART/SIO clock input/output pin ch0	
		310
UI0	UART/SIO data input pin ch0	310
UO0	UART/SIO data output pin ch0	310

# Interrupt Vector Index

IRQ0	External interrupt ch0289	)
IRQ0	External interrupt ch4289	)
IRQ1	External interrupt ch1289	)
IRQ1	External interrupt ch5289	)
IRQ2	External interrupt ch2289	)
IRQ2	External interrupt ch6289	)
IRQ3	External interrupt ch3289	)
IRQ3	External interrupt ch7289	)
IRQ4	UART/SIO ch0	
IRQ5	8/16-bit composite timer ch0 lower210	)
IRQ6	8/16-bit composite timer ch0 upper210	)
IRQ7	LIN-UART (Receive)	5
IRQ8	LIN-UART (Transmit)	5
IRQ9	8/16-bit PPG ch1 lower245	5
IRQ10	8/16-bit PPG ch1 upper245	5
IRQ12	8/16-bit PPG ch0 upper245	5
IRQ13	8/16-bit PPG ch0 lower245	5
IRQ14	8/16-bit composite timer ch1 upper210	)
IRQ15	16-bit PPG ch0271	
IRQ18	8/10-bit A/D429	)
IRQ19	Timebase timer131	
IRQ20	Watch prescaler/counter154, 169	)
IRQ22	8/16-bit composite timer ch1 lower210	)

CM26-10113-1E

### FUJITSU SEMICONDUCTOR • CONTROLLER MANUAL

F<sup>2</sup>MC-8FX 8-BIT MICROCONTROLLER MB95130/M Series HARDWARE MANUAL

November 2006 the first edition

PublishedFUJITSU LIMITEDElectronic DevicesEditedBusiness Promotion Dept.